# USB Based T3 E3 Basic Applications

**GL Communications Inc.**

# USB Based T3 E3 Analyzer

## T3 E3 Analyzer unit can work with a Desktop or with a Laptop PC

- Lightest (1.75 pounds) unit available in the market
- Small footprint, easy to carry in the pouch of a Notebook PC - perfect for air travel
- Cost Effective
- Connects to a PC via a USB 2.0 port
- T3, E3, T1, E1, interfaces supported. Ethernet interface will be supported in future
- Remote access for controlling and monitoring will be provided in future
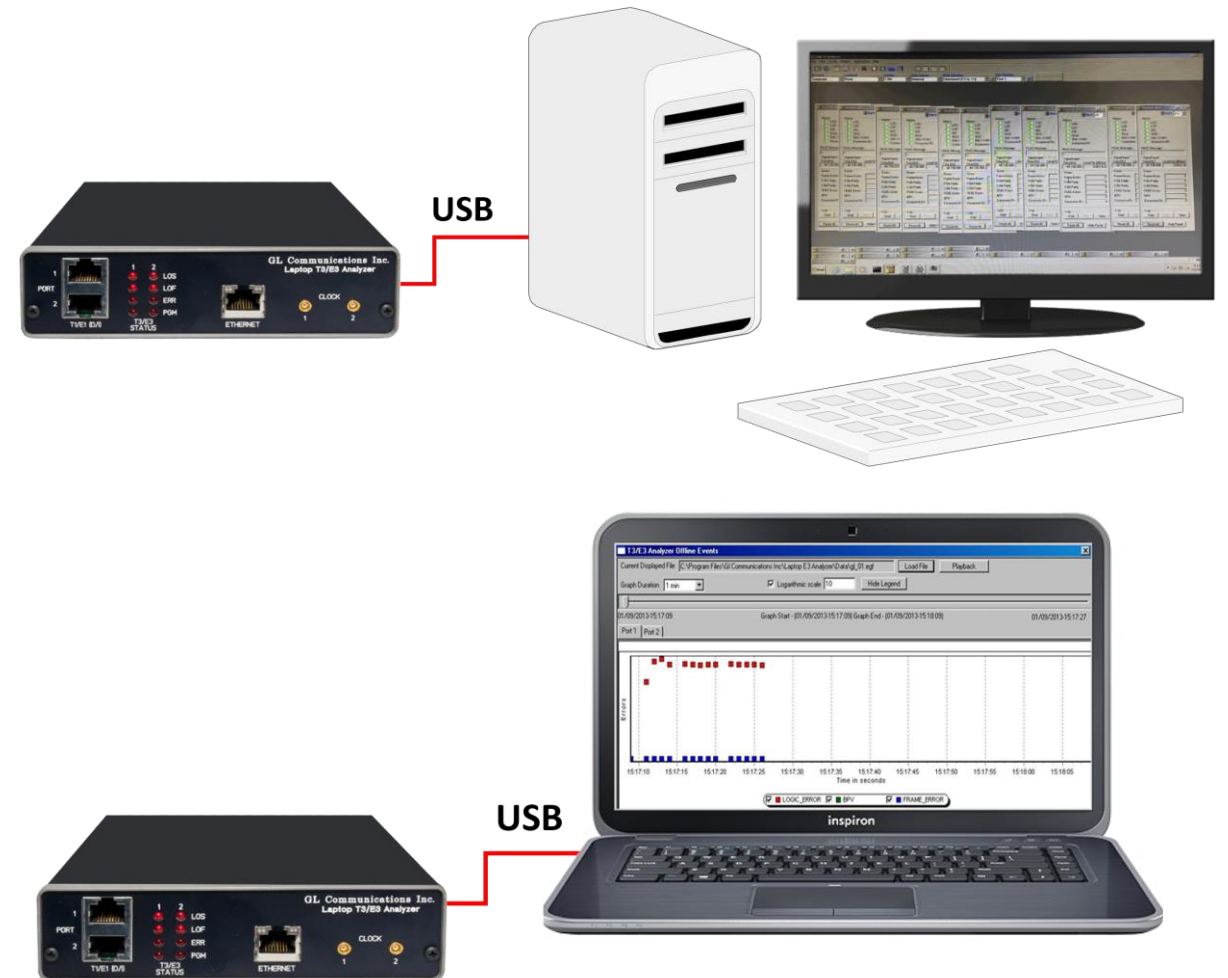
# Front and Rear Views of the Analyzer

- Used for installation, test, and troubleshooting of T3 E3 T1 E1 Ethernet lines

- Dual data stream capture capability

- Dropping and inserting T1 or E1

- Full Ethernet analysis

- HDLC, ATM, FR, and PPP analysis

- Used with GL's portable T1 E1 analyzer for individual T1, E1 analysis



**Front Panel**

**Back Panel**
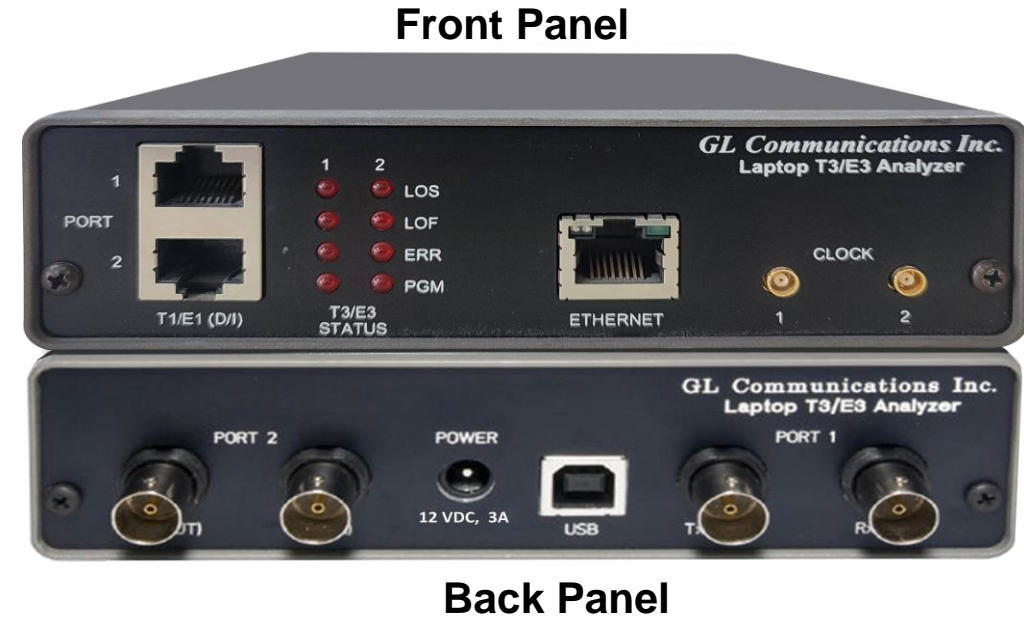
# Summary of Features & Benefits

- Software selectable T3 (DS3)/E3 interface along with T1 (DS1) and E1 Drop and Insert

- Dual T3 or E3 Receivers and Transmitters for non-intrusive and intrusive testing of both eastbound and westbound signals at the same time

- Simultaneously record/playback the entire T3 (DS3)/E3 in framed or unframed modes up to hard disk capacity

- Flexible clocking - internal, recovered (from T3 (DS3)/E3, T1 (DS1) or E1) and external

# Summary of Features & Benefits (Contd.)

- General T3 (DS3)/E3 signal testing capabilities

  - Alarms – monitoring and logging

  - Monitor T3 (DS3)/E3 frequency, line level and various errors.

  - Alarm generation and error injection

  - Decode and simulate Far End Alarm Channel (FEAC) messages.

  - T3 (DS3)/E3 error counters

  - Dual BERT and G.821 Analysis

- Scripting and automation through GL's Windows Client Server (WCS) approach

- Monitor/manage the analyzer remotely via Ethernet port

# Summary of Features & Benefits (Contd.)

- Channelized (Structured) Testing
  - ➢ Multiplex / De-multiplex T1 (DS1)/E1 signals (Drop and Insert)
  - ➢ Receivers for bidirectional monitoring with Dual T1 (DS1) / E1 drop
  - ➢ Transmit multiplexed externally inserted or internally generated T1 E1 streams into T3 (DS3) /E3
  - ➢ Stress test M13 (E13) multiplexers and 3/1 Digital cross connect systems
  - ➢ Dual channel drop and insert of T1 or E1 signals from any one of the T3(DS3)/E3 signals
  - ➢ Broadcast or loopback individual T1s/E1s within the T3 (DS3)/E3
  - ➢ Generates 28 T1s or (21 E1s) signals within the T3 (DS3) or 16 E1s within E3 output
- Unchannelized (Unstructured) Testing
  - ➢ WAN Testing
  - ➢ Protocol testing for ATM, PPP, HDLC, and Frame Relay
  - ➢ Transmit / Verify HDLC frames with user defined headers

# Basic Applications

- Bit Error Rate Test (BERT)

- Loopback Modes, Clock, Framing Formats, Structured/Unstructured Modes

- Transmit and Receive Configuration

- Monitor T1 or E1 Frames over T3 or E3 Lines

- Alarm Generation and Error Injection

- Tx Rx Memory Loopback

- Monitor Received Data

- Multiplex and De-multiplex T1 or E1 signals

# Loopback Modes, Clock, Framing Formats, Structured/Unstructured Modes

E3 Interface Configuration Parameters
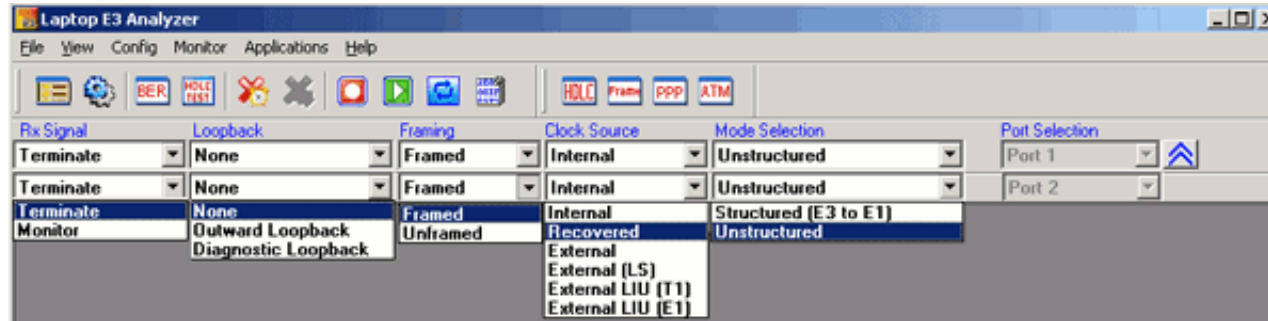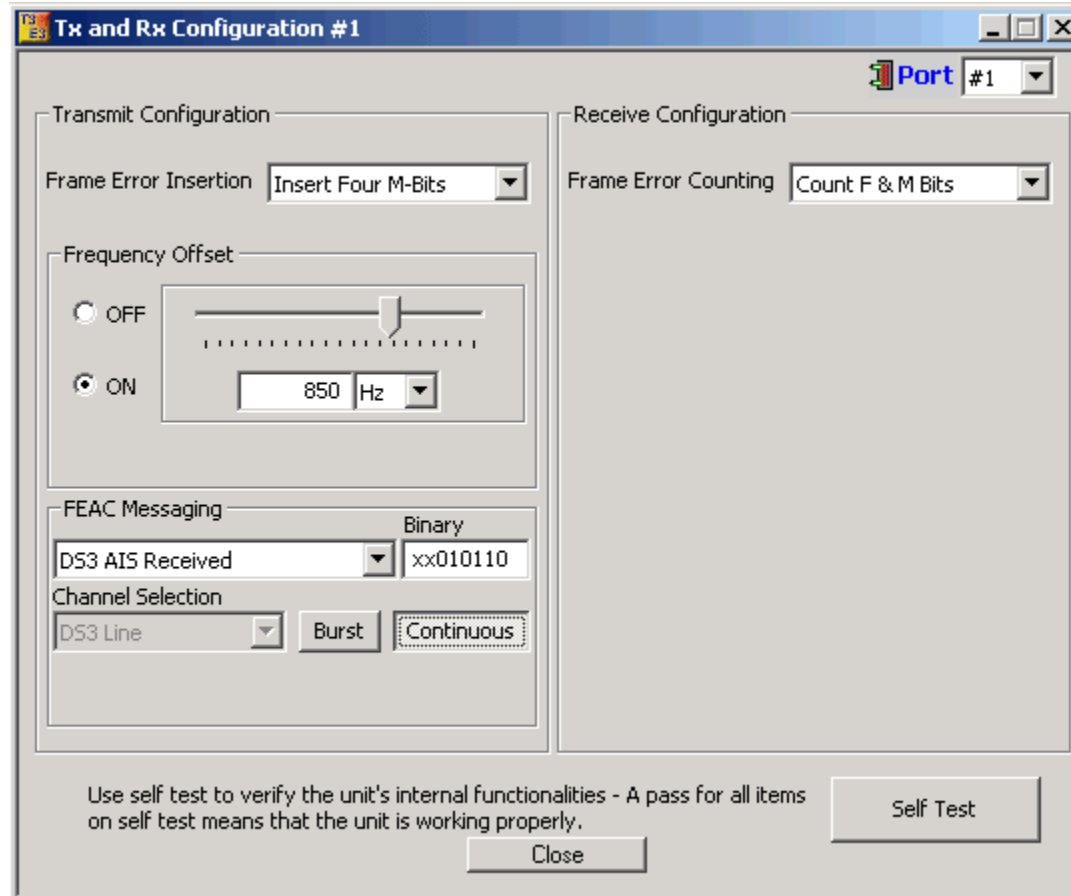


T3 Interface Configuration Parameters
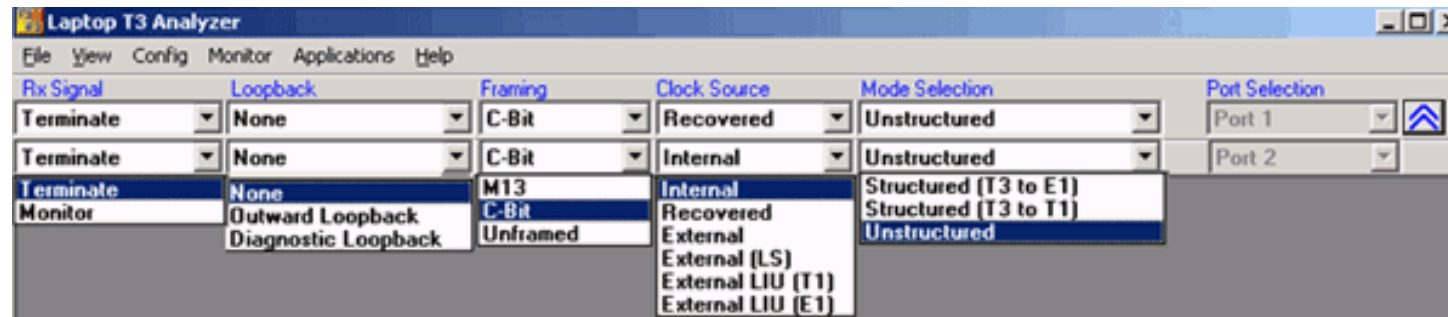
# Transmit and Receive Configurations

**Tx/Rx parameters for the T3 signal**



**Tx/Rx parameters for the E3 signal**

# Transmit and Receive Configurations (Contd.)

- Possible frame error insertions in T3
  - ➢ Single FAS word (1111)
  - ➢ Single FAS word (0000)
  - ➢ Four FAS words (1100)
  - ➢ Four FAS words (0011)
- Possible frame error insertions in T3
  - ➢ Single F Bits
  - ➢ Single M Bits
  - ➢ Four F Bits
  - ➢ Four M Bits
- Frequency Offset  ranging from +50 to -50 ppm for the internal clock source
- Standard and User-defined FEAC Message transmission (only for T3 Systems with C-Bit Parity Framing Format)
- Frame Error Counting
  - ➢ E3 - Bit Errors (FAS), Word Errors (FAS)
  - ➢ T3  - F & M Bits , F Bits , M Bits
- Self Test the unit

# Transmit and Receive Configurations (Contd.)

## FEAC Message (only for T3 Systems with C-Bit Parity Farming Format)

- Using the FEAC channel, alarm or status information from the far-end terminal can be sent back to the near-end terminal

- The Monitor T3 Line indicates the incoming FEAC message

# Alarm & Error Display for T3 (DS3) & E3



**T3 Monitoring**          **E3 Monitoring**

# Alarm and Error Display for T3 (DS3)

- Available alarms are –
  - LOS - (Loss of Signal)
  - LOF - (Loss of Frames)
  - AIS - (Alarm Indication Signal)
  - Idle
  - RAI/X-Bit
  - Excessive 0's
- Error Indications
  - Frame
  - P- Bit parity
  - C-Bit parity
  - FEBE
  - BPV
  - CV
  - Excessive zeros

# Alarm Generation and Error Injection
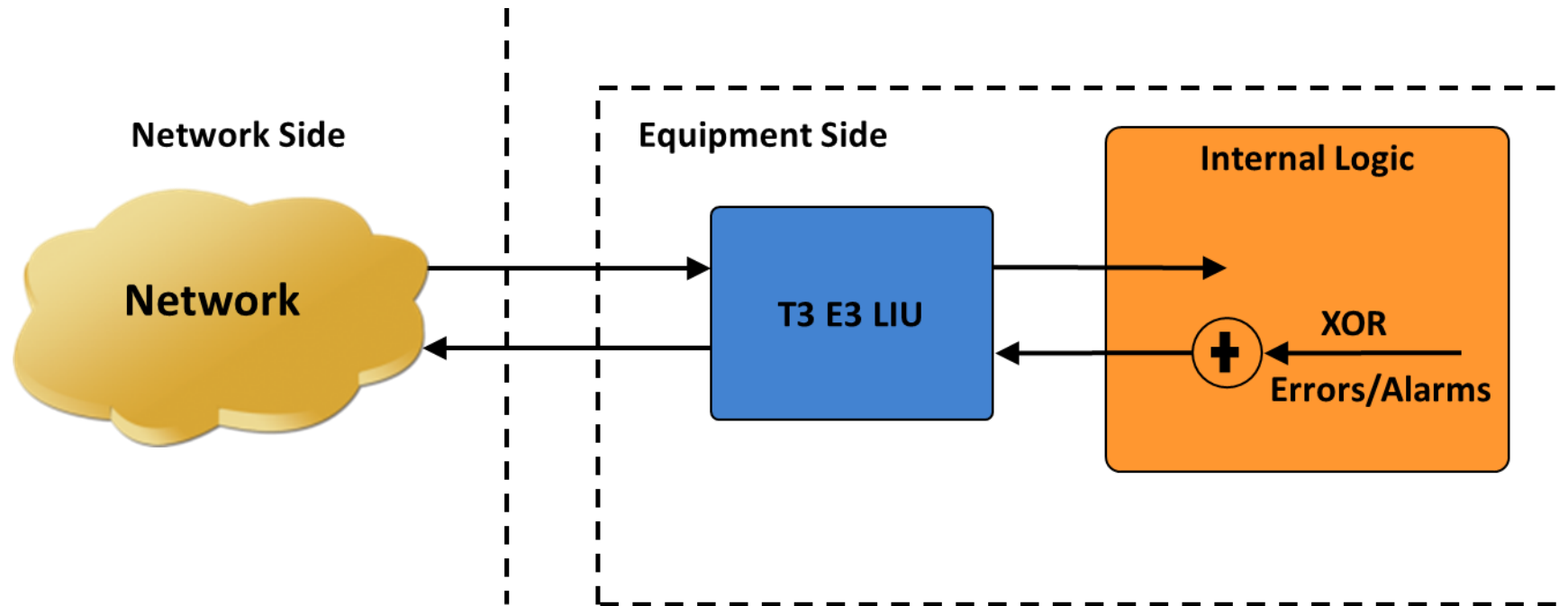


- Internally generates various types of errors and / or alarms and transmits them on the outgoing T3 (DS3)/E3 stream
- Automatically inserts single bit errors or at regular intervals of time (secs)

# Alarm Generation and Error Injection (Contd.)



- Alarms - LOS (Loss of Signal), LOF  (Loss of Frames), AIS (Alarm Indication Signal), Idle, RAI/X-Bit, Remote Alarm Indication (RAI)
- Errors – Frame, P-Bit Error (T3 Only), C-Bit Error (T3 Only), FEBE Error (Far End Block Errors) (T3 Only), BPV - BiPolar Violation (T3 Only), Excessive 0's, CV Errors (E3 Only)
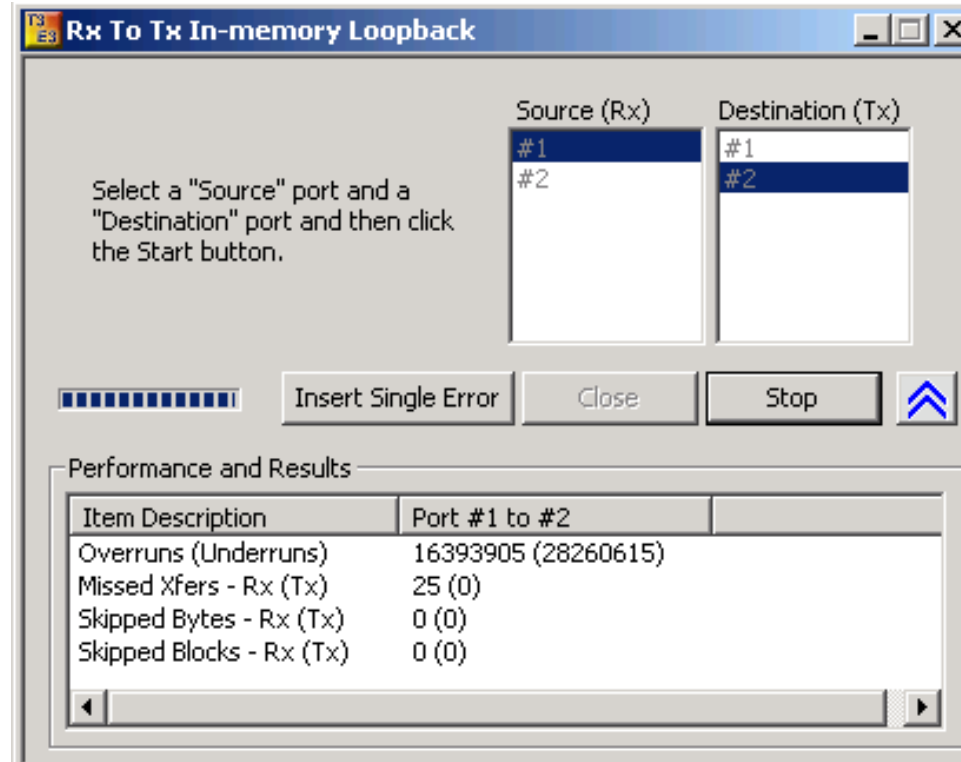
# Tx Rx Memory Loopback

Logical Diagram for Transmit and Receive Memory Loopback for T3 (DS3)/E3 Analyzers
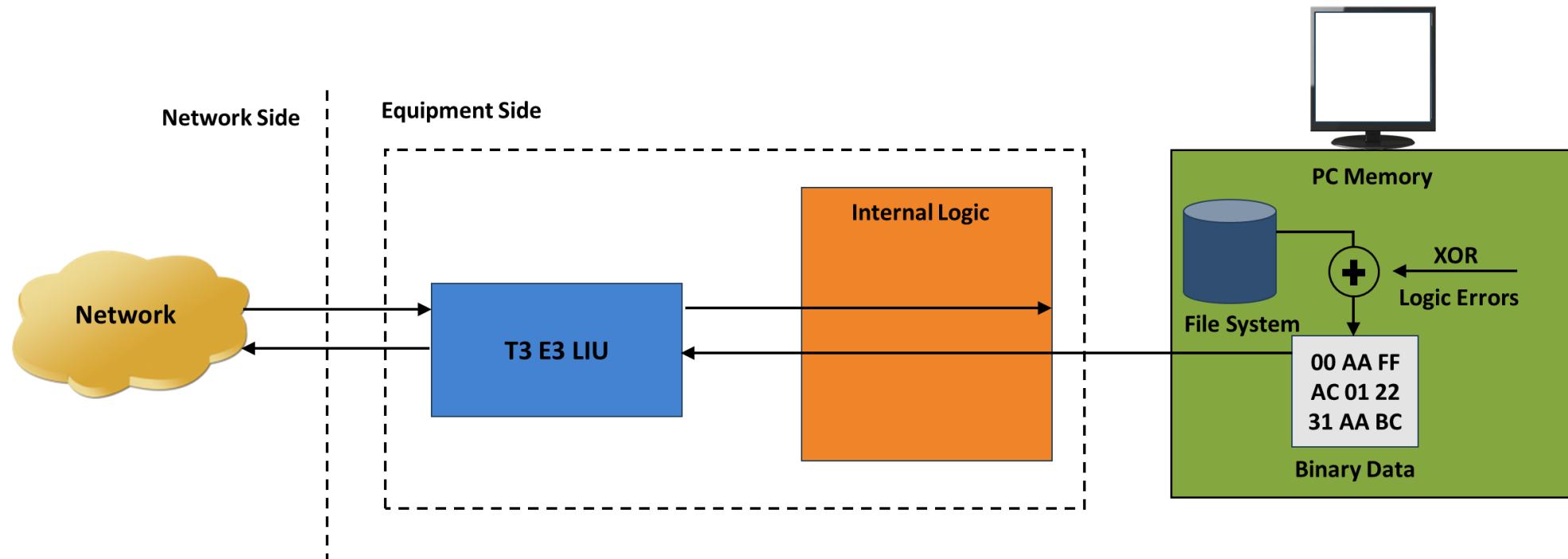


- With the loopback, the data received from the network is retransmitted back via the PC memory
- Optionally logic errors (XOR) can be inserted into the loopback stream during loopback
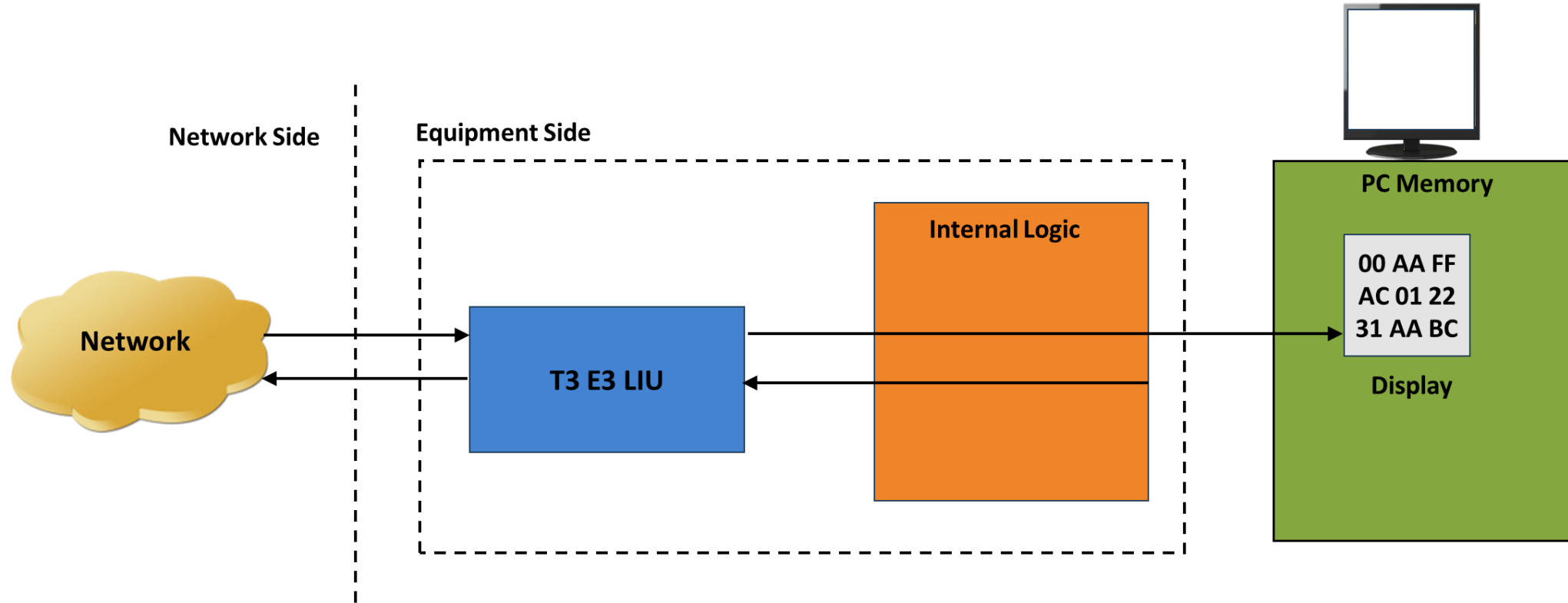- Allows insertion of single bit errors manually

# Tx Rx Memory Loopback (Contd.)



- Used for diagnostic purposes
- Memory Loopback and Bit Error Rate Test applications can be run on two different ports simultaneously to verify the operation of the analyzer unit
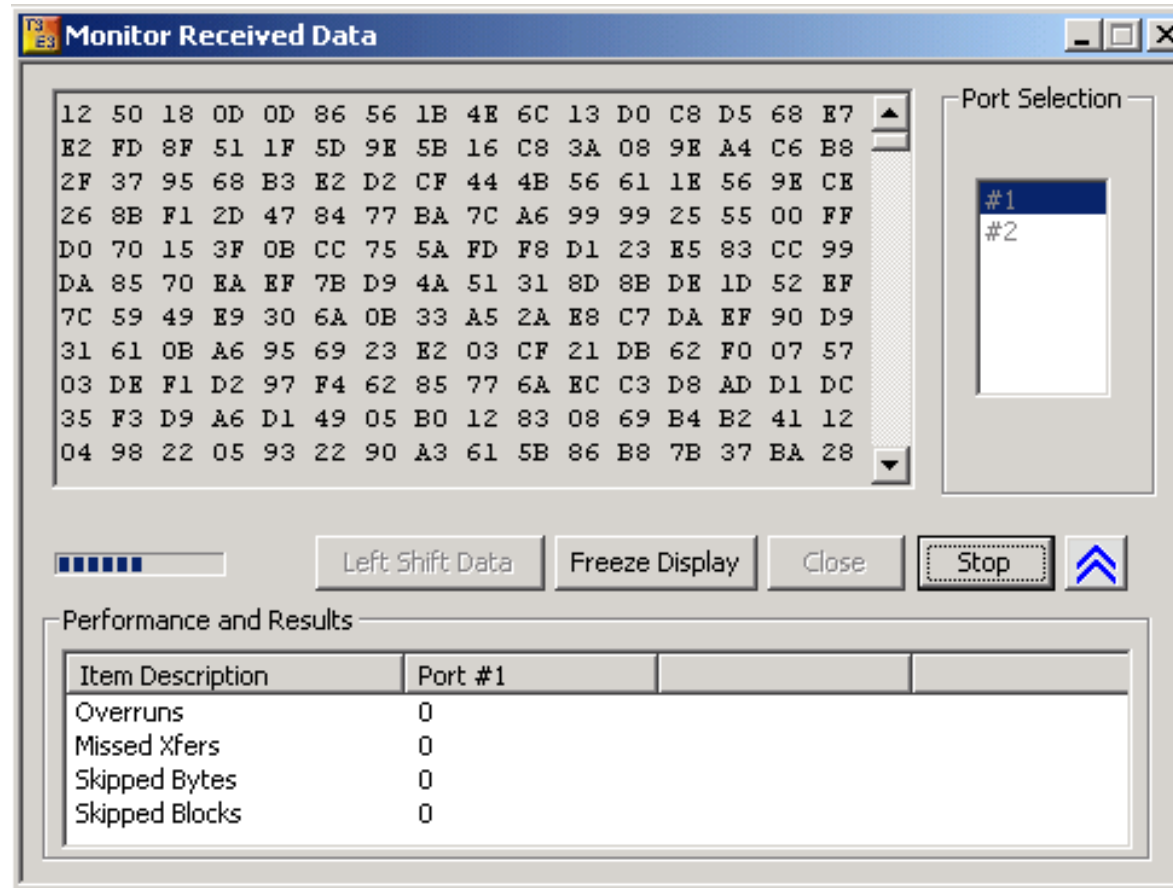
# Monitor Received Data

Logical diagram for the Monitor Received Data application



- This application can monitor raw bit values on the selected ports. The raw bytes received from the network at the T3 interface are monitored and displayed on the selected ports
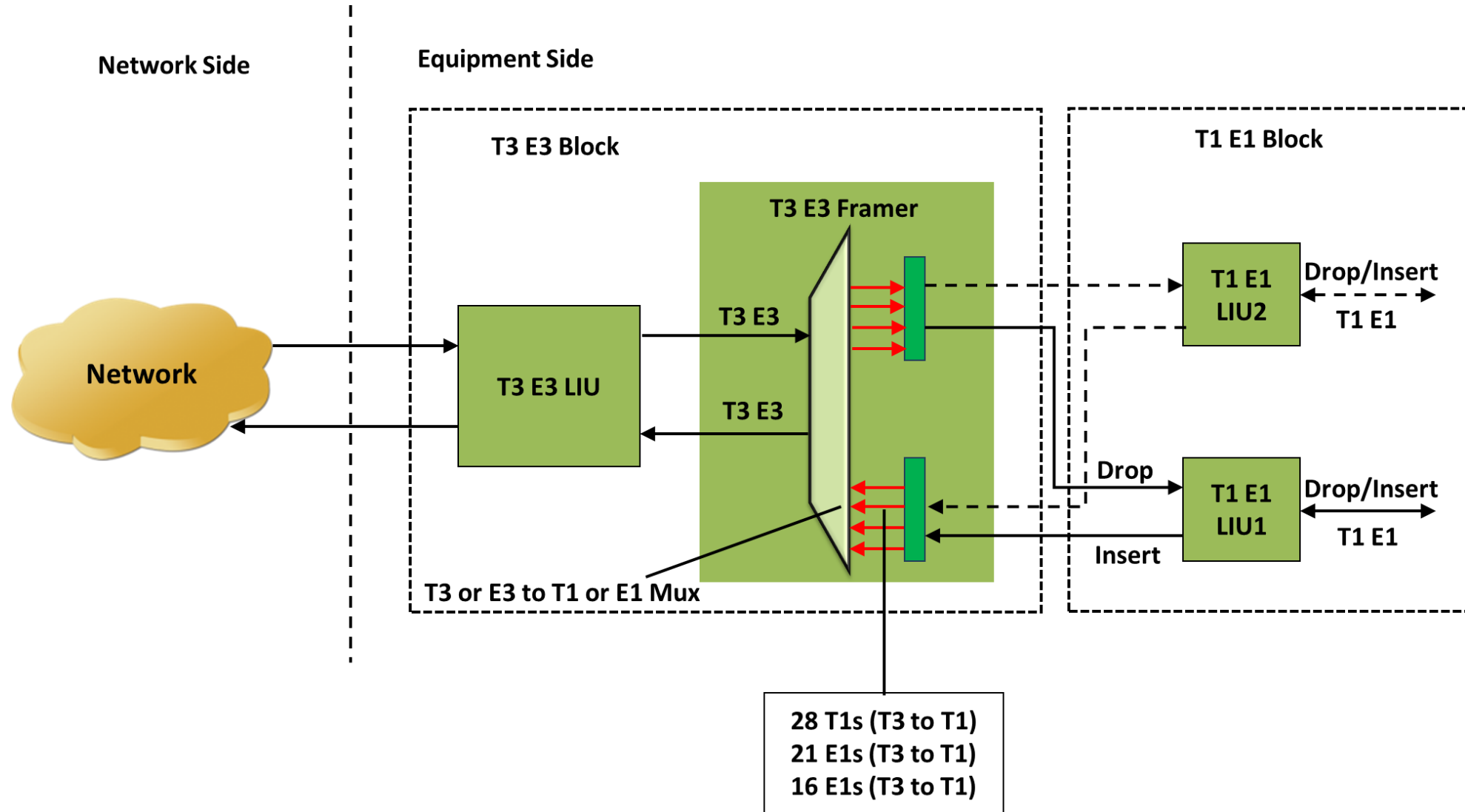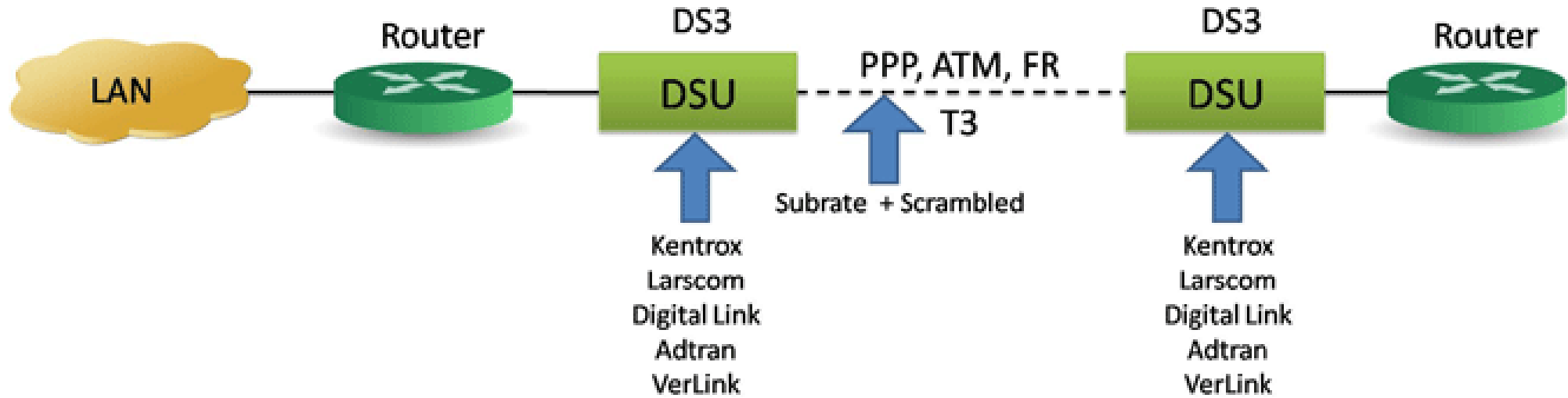
# Monitor Received Data (Contd.)



- Used for quickly testing the byte alignment of the received data
- Underruns, MissedXfer, Skipped Bytes, and Skipped Blocks display provides the receive data pipe performance
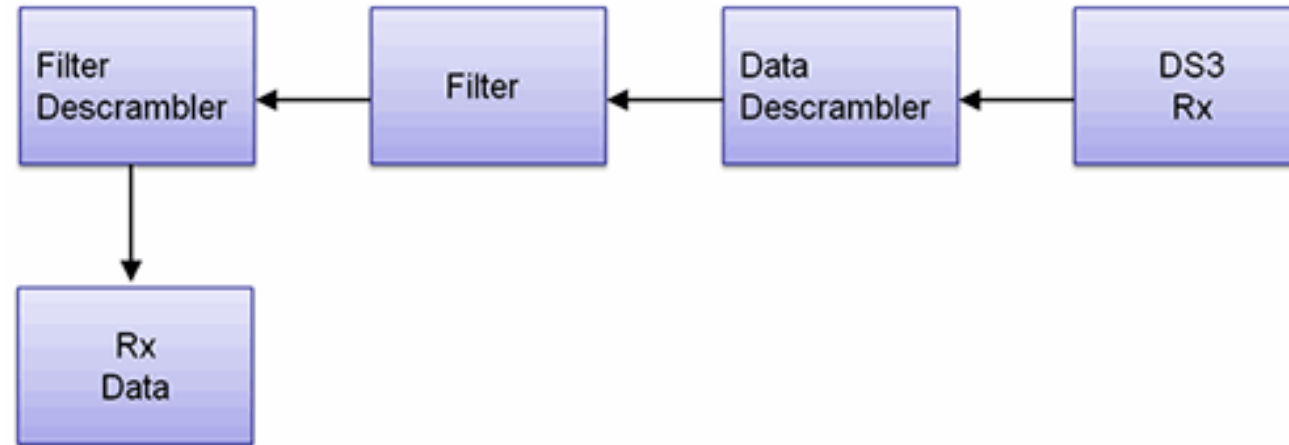
# Multiplex and De-multiplex T1 or E1 signals

Logical Diagram for Drop and Insert Structured Mode



28 T1s (T3 to T1)
21 E1s (T3 to T1)
16 E1s (T3 to T1)

# T3 (DS3) Subrate and Scrambling



LAN — Router — DS3 DSU — PPP, ATM, FR / T3 / Subrate + Scrambled — DS3 DSU — Router

Kentrox
Larscom
Digital Link
Adtran
VerLink

Kentrox
Larscom
Digital Link
Adtran
VerLink

# DS3 Subrate Block Diagram

# Auto Config
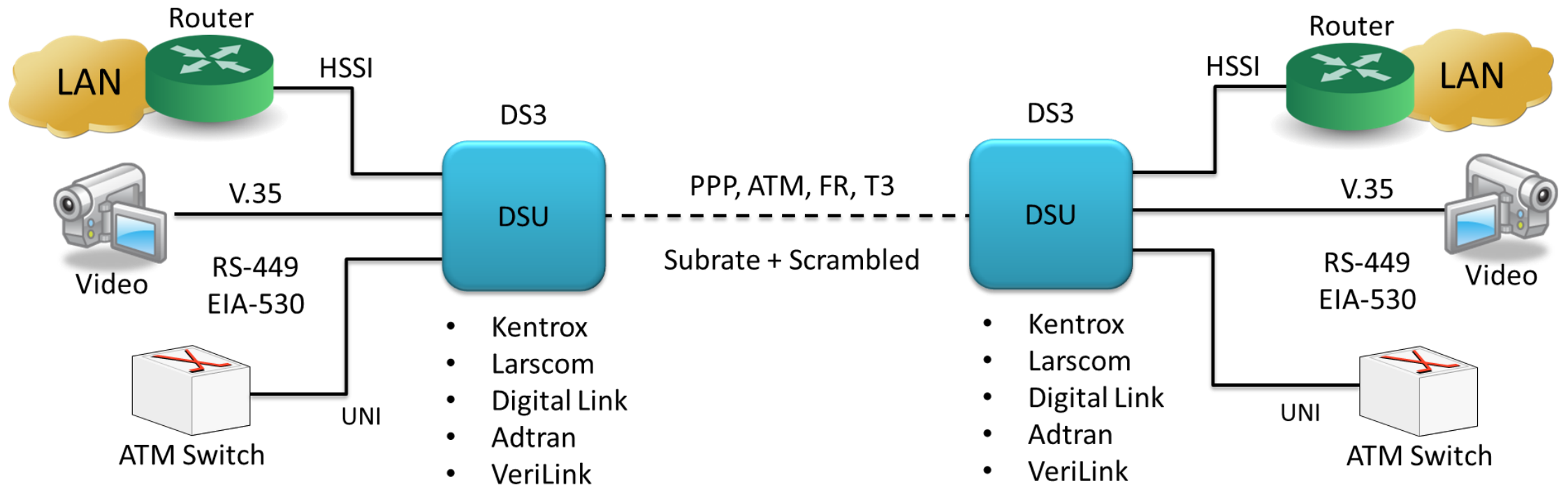
# DS3 Subrate Configuration Setup
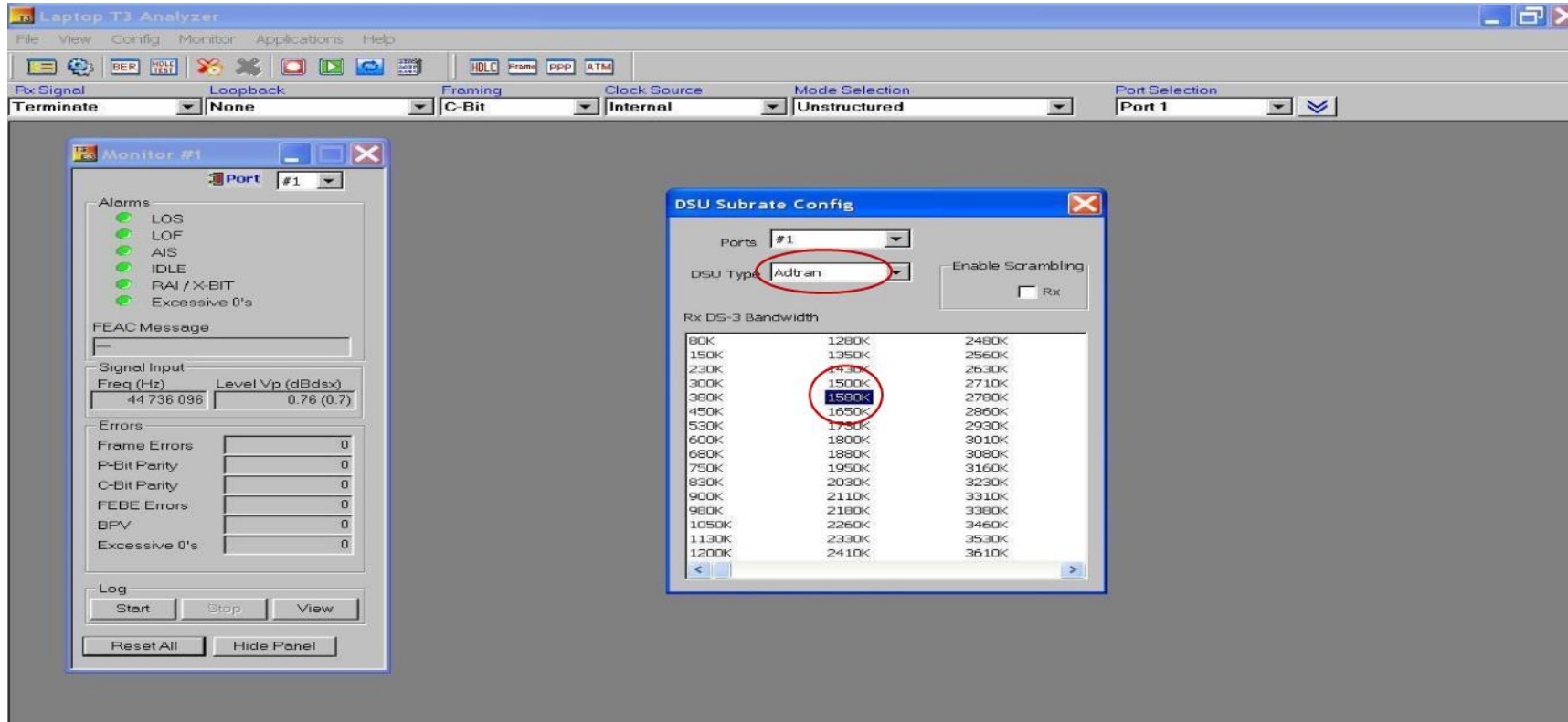


- The user has the ability with the USB T3 E3 unit to configure the DSU and the rate using the DS3 Subrate Config window as shown in the screen capture

# Scrambling and Subrate



- For Data, Packetized Voice, and Video and other Unchannelized Uses
- Generally, not for 28 T1s

# DSU Types



Digital Link Subrate

Larscom Subrate

Verlink Subrate

Adtran Subrate

# T3-T1



**Two T-taps with Attenuator**

T3

**tProbe™ T1 E1 Analyzer**

**T1 Drops**

**T3 Analyzer Unit**

**ISDN CAS**

USB

USB

Notebook PC

# Multiplex and De-multiplex T1 E1 Signals

User interface for the Structured Mode (Drop / Insert) Settings
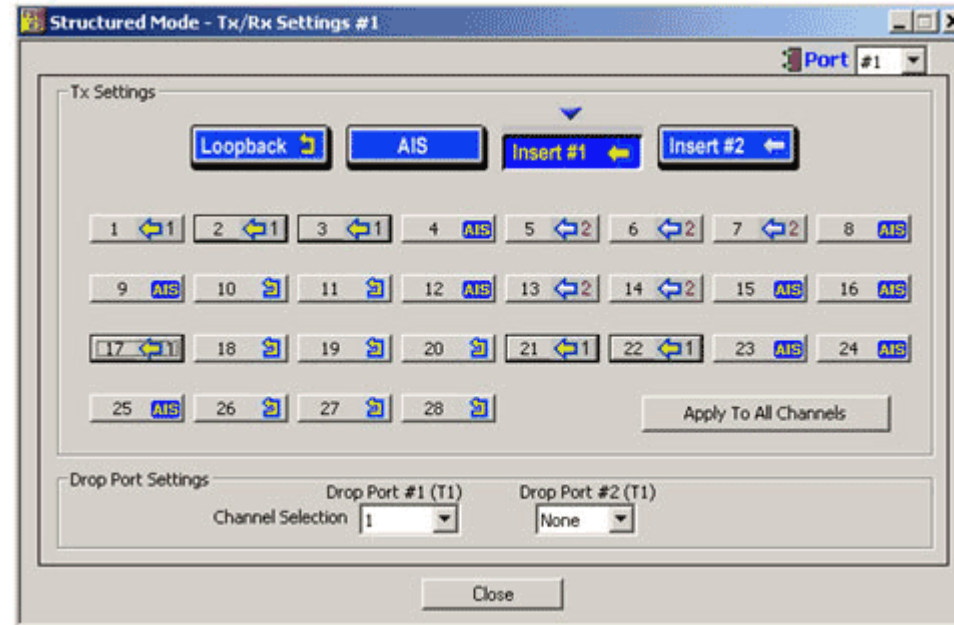


- Up to two user selected T1 (or E1) channels can be externally inserted using the T1 E1 input/output interface into any one of the transmitted T3 (DS3) or E3 signal
- The inserted T1 or E1 signal can be selectively transmitted through one or more of the T1 E1 transmit channels or broadcasted through all the T1 E1 channels
- Up to two user selected T1 or E1 channels can be dropped

# Bit Error Rate Test - BERT
# (Full Frame & Unframed)
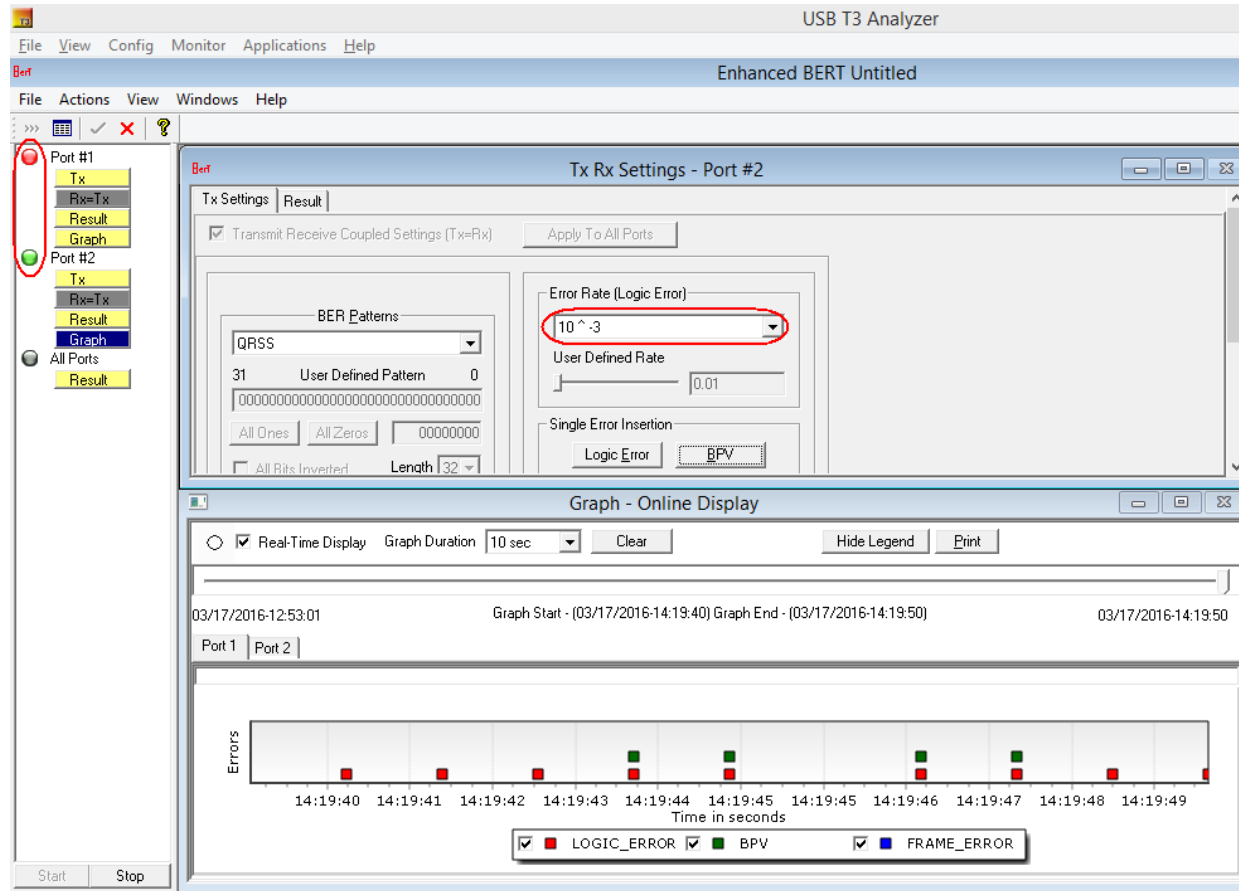


- GL's T3 E3 Bit Error Rate Tester application measures the correctness of data received on T3 E3 channels for a repetitive fixed or pseudorandom pattern for the given transmission
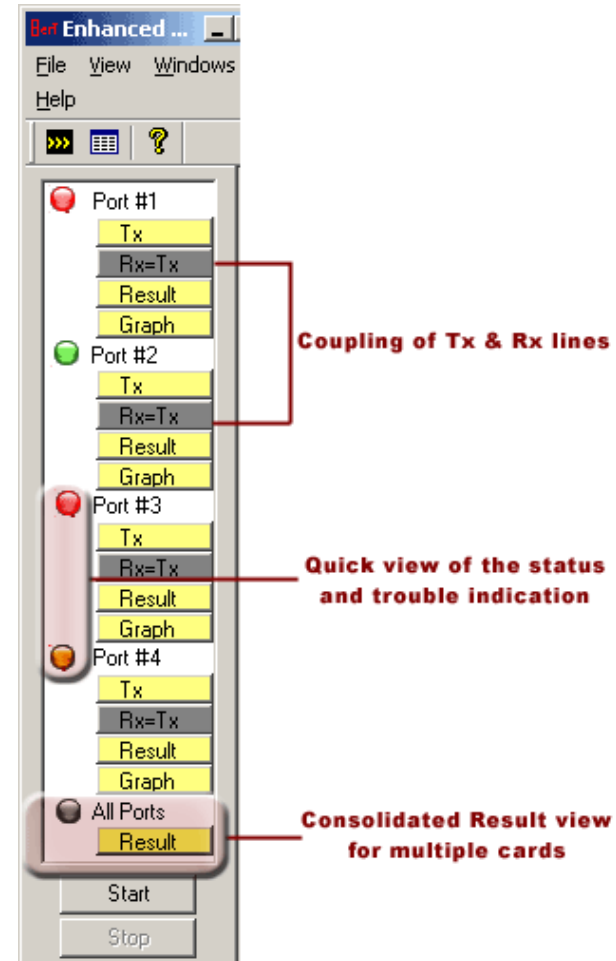
# Selection of Port – View Error Status, Results

## Bit Error Rate Test - BERT

- Quick view of the status and trouble indication

- Supports testing on multiple ports simultaneously with consolidated result view

- Tx and Rx settings for multiple ports can be independently controlled or they can be coupled (Apply to All) from a single card to all cards

# Error and Bit Patterns Insertion
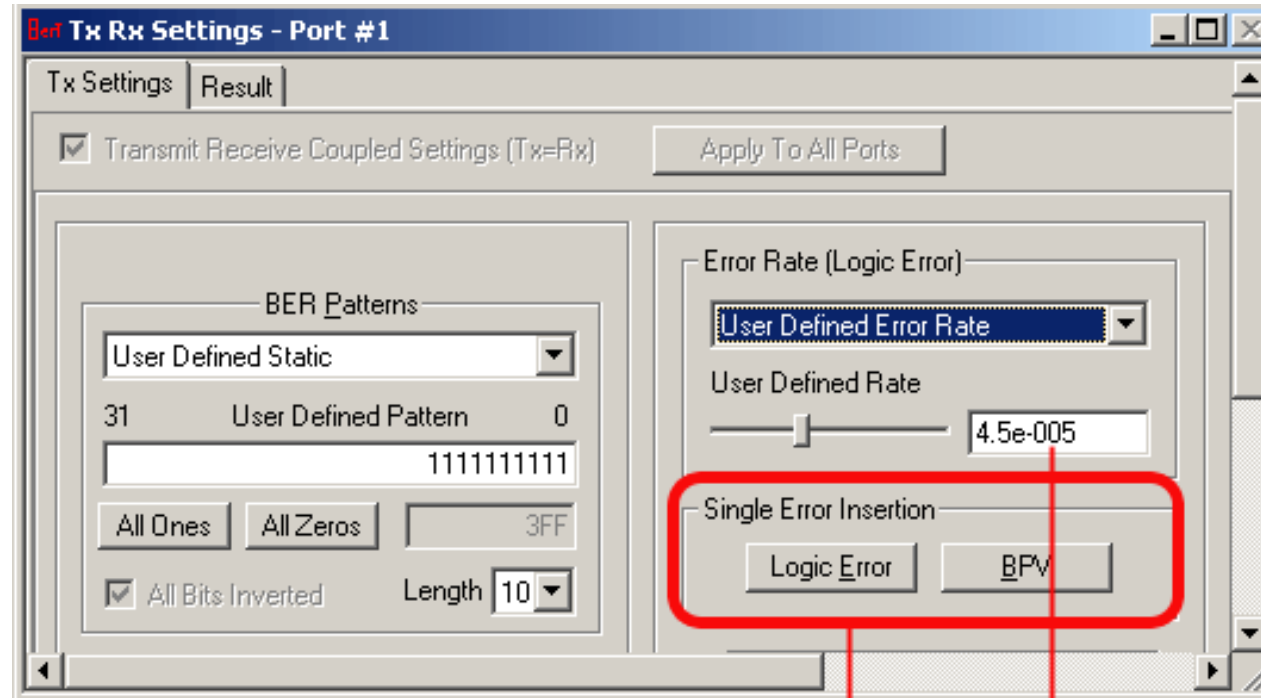

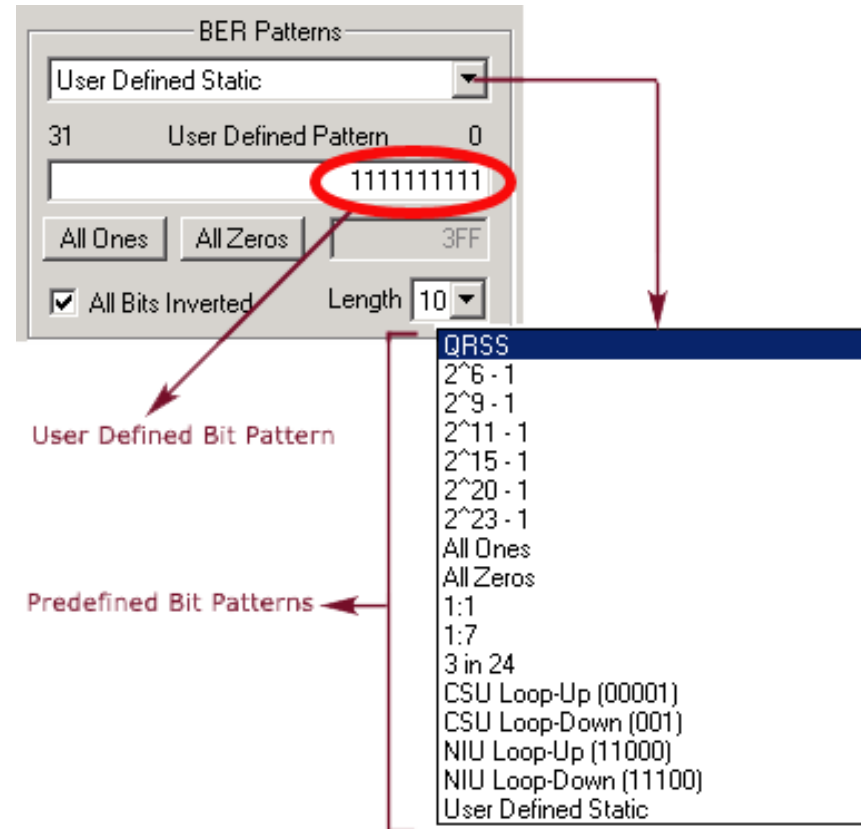
- Supports pre-defined and user defined error insertion rate ranging from 10^-2 to 10^-9 (0.01 to 1e-009)

- Automatic insertion of Logic and BPV errors at regular intervals of time (secs) or just insert single bit errors into the transmit stream

# Static and User-Defined Pattern Selection



- Generates standard static bit patterns such as - QRSS, 2^5-1, All ones, All zeros, 1:1, CSU Loop-Up (0001), CSU Loop-down (001), NIU Loop-UP (11000), NIU Loop-Down (11100), and more
- Generates user-defined static patterns of size up to 32 bits

# Graphical Result
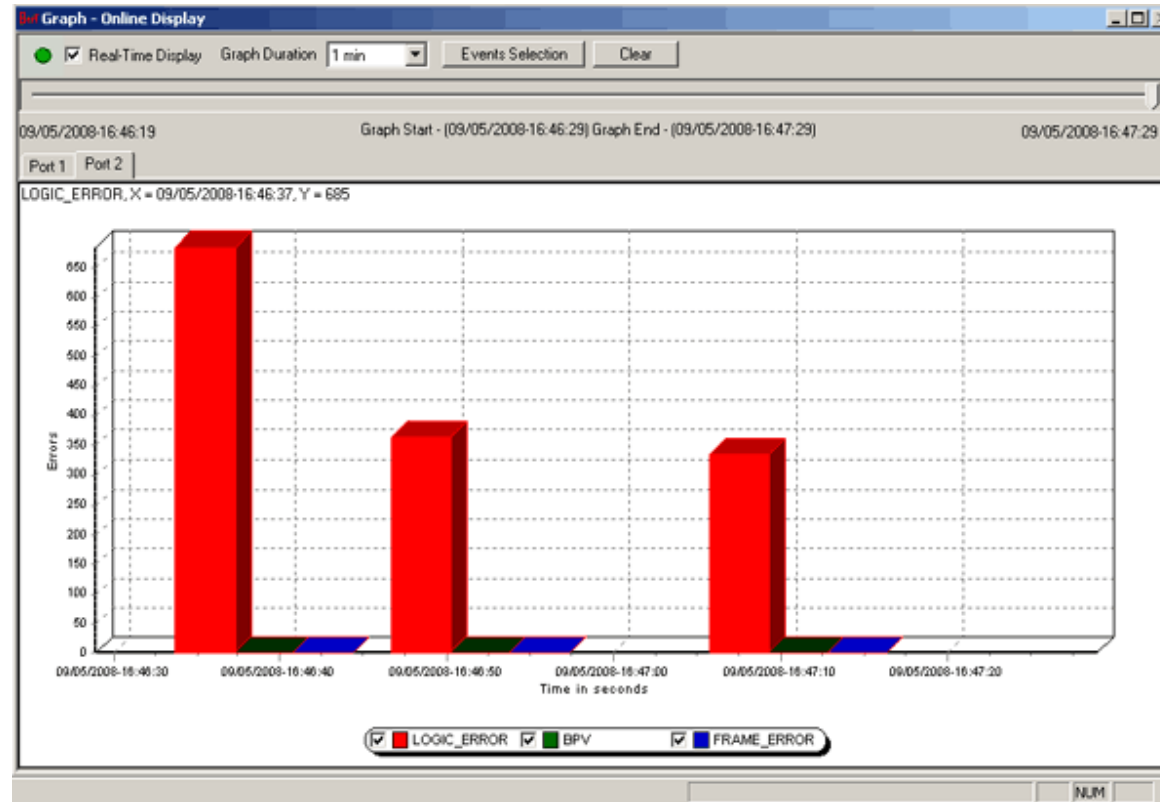


- The Error Count Vs Time graph of the bit error test results is displayed
- For real-time graph, the predefined or the user defined bit pattern and the errors can be inserted
- Offline graph display the saved (*.xml) files are loaded for analysis
- Any of the events such as LOGIC_ERROR, BPV, or FRAME_ERROR can be set for the display

# Thank you