LightSpeed1000™
OC-3 / STM-1 and OC-12 / STM-4
ATM and PoS Analyzer

(Legacy Product)

◇GL Communications Inc.
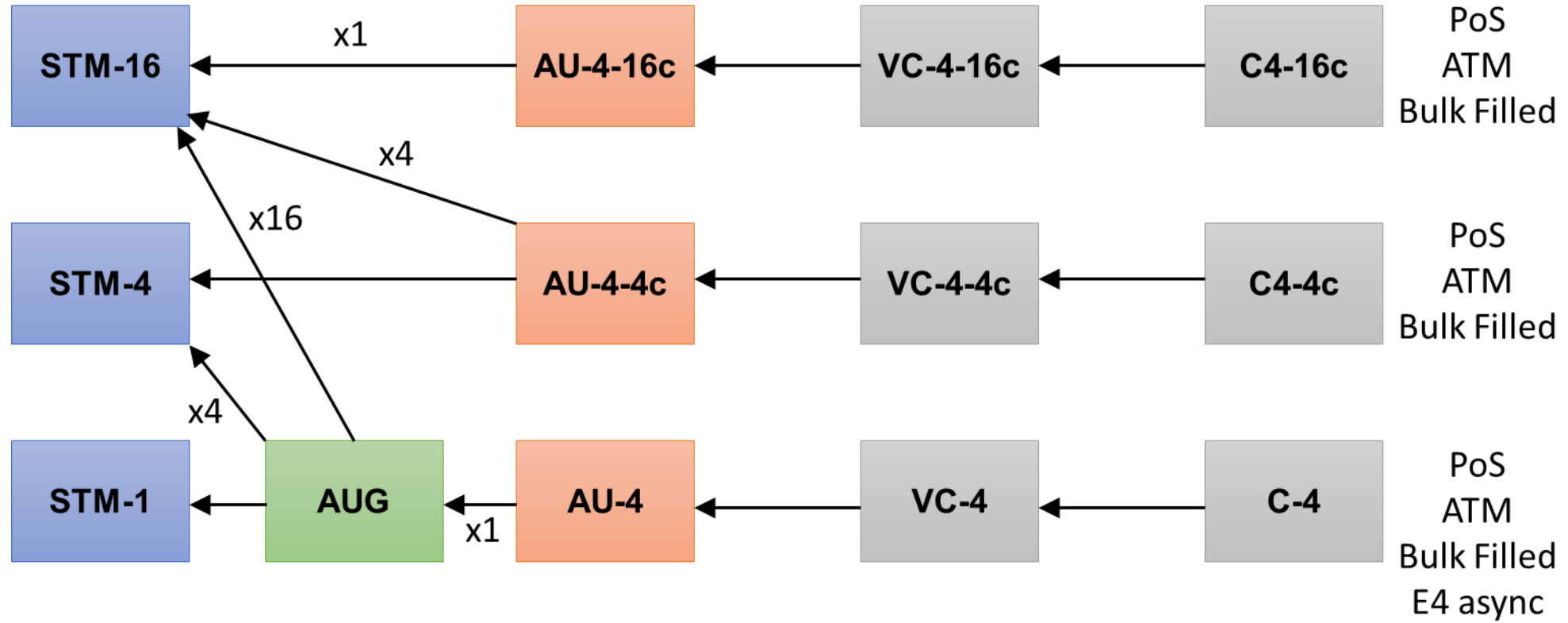
Synchronous Signal Capacity

- STS – Synchronous Transport Signal
- OC – Optical Carrier
- STM – Synchronous Transport Module

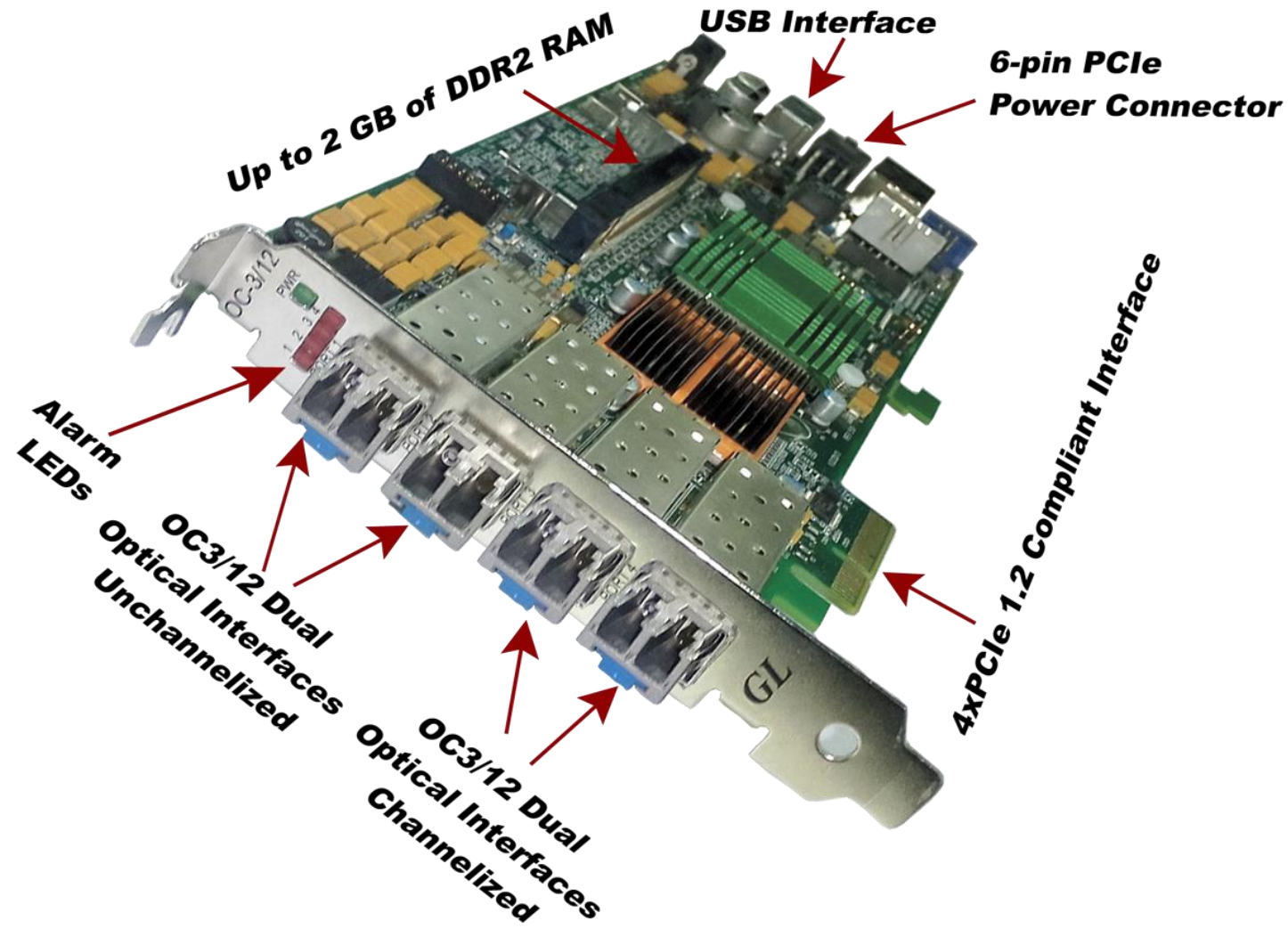| SONET Rates	Optical	STM Level	Bit Rate
STS-1	OC-1	STM-0	51.84 Mbps
STS-3	OC-3	STM-1	155.52 Mbps
STS-12	OC-12	STM-4	622.08 Mbps
STS-24	OC-24	STM-8	1.244 Gbps
STS-48	OC-48	STM-16	2.488 Gbps
STS-192	OC-192	STM-64	9.953 Gbps

SONET Payload Mapping
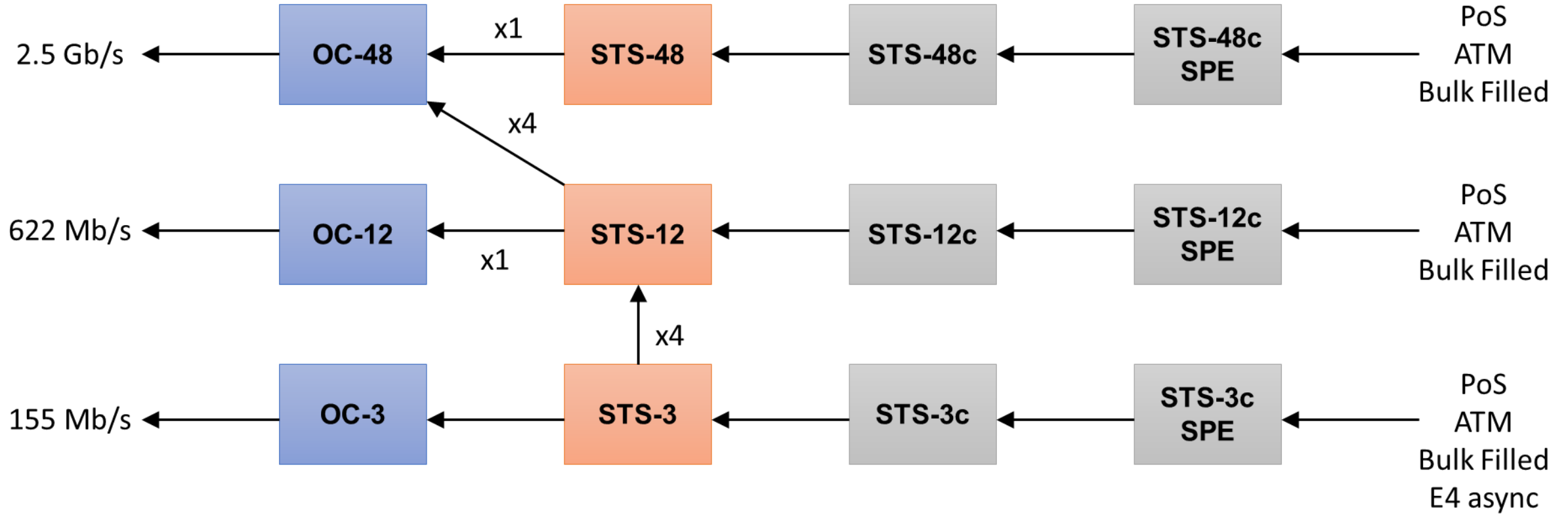
SDH Payload Mapping

Portable OC-3 / STM-1 and OC-12 / STM-4 Analysis Unit

Dual OC-3/12 and STM-1/4 PCI-Express Card

Up to 2 GB of DDR2 RAM

USB Interface

6-pin PCIe Power Connector

4xPCIe 1.2 Compliant Interface

Alarm LEDs

OC3/12 Dual Optical Interfaces Unchannelized

OC3/12 Dual Optical Interfaces Channelized

Hardware Interfaces

FRONT PANEL

PWR

1 2 3 4

Port #1   Port #2   Port #3   Port #4

GL Communications Inc.
LightSpeed 1000

Alarm
LEDs

OC-3 /STM-1 OC-12/STM-4
Dual Optical Interfaces
Unchannelized

OC-3 /STM-1 OC-12/STM-4
Dual Optical Interfaces
Channelized

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RJ-45
Interface

USB

POWER

12 VDC, 1A

External Clock
Interface

USB Jack

Power Jack

REAR PANEL

Supported Protocols

- ATM
  - ➢ ATM Forum User Network Interface Specification
  - ➢ ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432

- PPP over SONET (PoS)
  - ➢ Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615 (1619) / 1662 of the PPP Working Group of the Internet Engineering Task Force (IETF)

- OC-3/OC-12/STM-1/STM-4 Transparent Payload
  - ➢ Analyzer processes SONET/SDH payload in transparent (RAW) mode without any transport protocols

- Channelized access for T1 E1 T3 E3
  - ➢ For processing ISDN, SS7, CAS and other channelized protocols
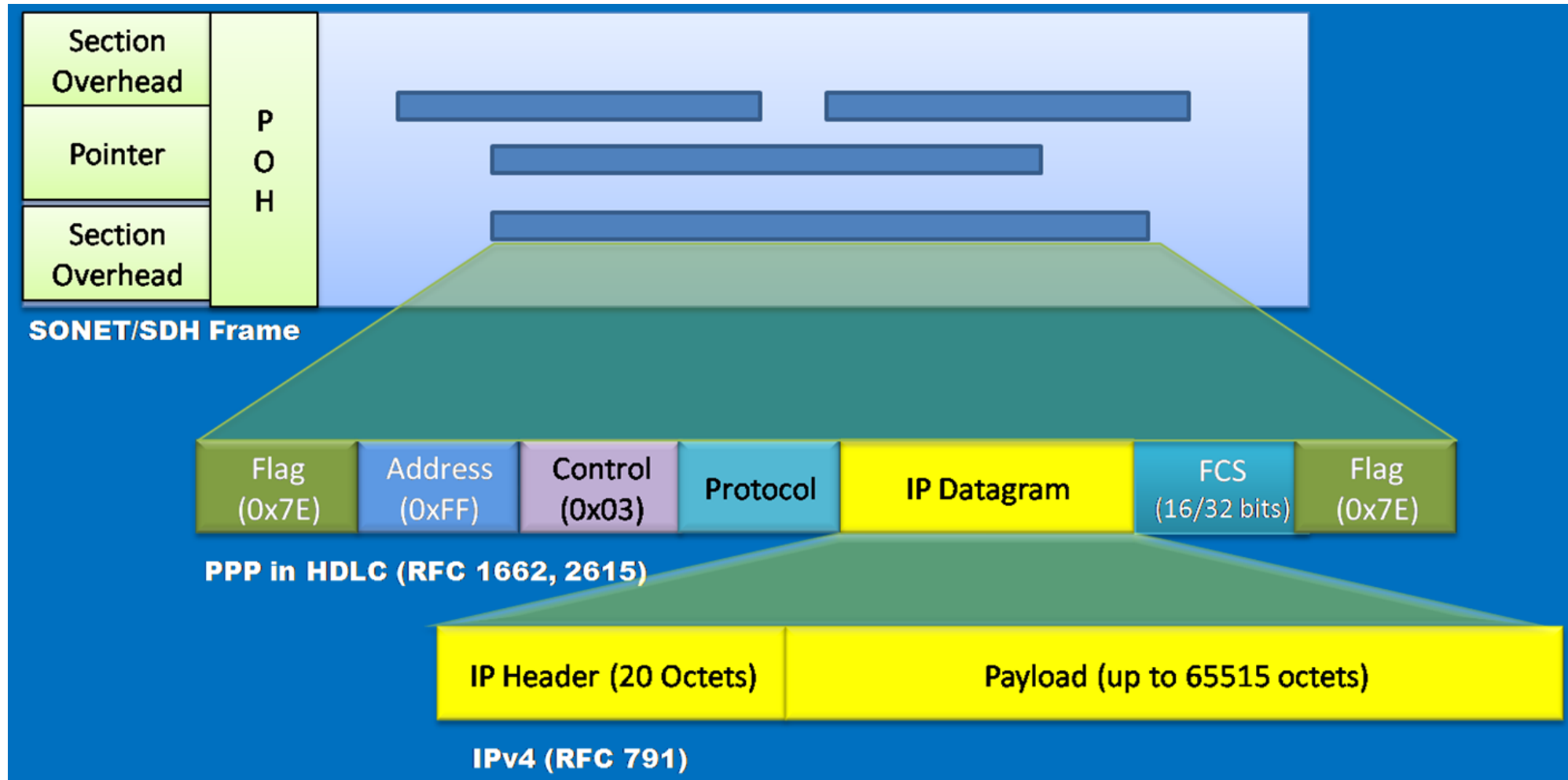
Features

- Wire-speed processing of ATM, PoS or RAW data for Tx and Rx for both ports

- Software selectable OC-3(STM-1) or OC-12(STM-4) for ATM, PoS or Transparent Traffic

- Ability to capture/playback to/from disk at full rate in both directions for both ports

- Comprehensive transmit / receive test capabilities; transmitting and verifying data with incrementing sequence numbers

- Detailed offline analysis that is not possible with other test instruments

- Simultaneous synchronous capture is possible on multiple boards. The captured file can be played back to reproduce the traffic

- Industry proven Protocol Analyzer for ATM (AAL2, AAL5), UMTS, PPP (IP and higher layer protocols)

- Easy to use and flexible Bit Error Rate Test (BERT) application for ATM, POS, and RAW

- Complex and flexible hardware based filtering options: sixteen 128 bit independently filters with bit masks, for both ports with AND/OR include/exclude conditions

Features (Contd.)

- Hardware based precise time-stamping of cells / packets with 10 nsec resolution, 1 ppm accuracy

- Single mode or multi mode SFP support

- High performance x4 PCIe interface with optimized DMA to perform rx and tx packets to/from PC memory

- Precisely emulates packet delays that occur over SONET/SDH carrying ATM or PoS traffic, delay is adjustable from 1 ms to maximum of 500 mSec

- Flexible DMA circular buffer architecture to read and write cells and packets at wire-speed

- Multiple cards per system for super high capacity monitoring and test system

- API Toolkit to develop user specific applications

- Optional onboard SODIMM memory (DDR2) – up to 2 Giga bytes; Field upgradable firmware

- Hardware independent of higher level protocol for easy adaptation of future protocols

- Supports MS-Windows® and Linux operating systems

PoS - Packet over SONET / SDH

- IP packets mapping into SONET / SDH payloads

Section Overhead		
Pointer	P O H	
Section Overhead		

SONET/SDH Frame

| Flag (0x7E) | Address (0xFF) | Control (0x03) | Protocol | IP Datagram | FCS (16/32 bits) | Flag (0x7E) |

PPP in HDLC (RFC 1662, 2615)

| IP Header (20 Octets) | Payload (up to 65515 octets) |

IPv4 (RFC 791)

PoS - Packet over SONET / SDH

IP packets mapping into SONET / SDH payloads

- IP packets mapping into SONET / SDH payloads

- Apply 20 bytes IP header for each IP packet

- PPP packet headers and HDLC framing are applied to each IP Datagram

- Frame check sequences (FCS) and octet stuffing are appended to the IP Datagram

- Idle flags are inserted in between frames (IP Packets)

- Final scrambling of the IP Datagram and synchronous mapping by octet into the SONET/SDH frame

PoS Analyzer Features

- Supports signal rates of 155.52 Mbps for OC-3 and 622.08 Mbps for OC-12 interface

- Capture and analyze Point-to-Point Protocol (PPP) over SONET/SDH as per RFC 2615

- Wire speed cell generation and processing on single or multiple ports using internal logic

- Supports payload scrambling of polynomial $1+X^{43}$

- Supports up to sixteen128 bits hardware filters. All filters are protocol independent and provide a greater flexibility. Deep packet inspection becomes easier with support of filter offset feature.

- SONET Statistics: Link State, Line Speed, Section LOS, Section LOF, Section BIP (B1), Line AIS, Line RDI, Line REI (FEBE), Line BIP (B2), Path AIS, Path RDI, Path REI (FEBE), Path BIP (B3).

- Packet statistics: Tx/Rx Byte Count, Tx/Rx Packet Count, Rx FCS Error Count, Rx Abort Packet Count, Rx Minimum and Maximum Packet Length Violation Error Count

PoS Analyzer Features (Contd.)

- IP Statistics supported: IP Packets Received, IP Checksum Errors, UDP data over IP Layer frame count

- Loopback options: Rx-to-Tx memory loopback, line loopback, diagnostic loopback, and PL3 loopback options

- Bit Error Rate Test module supports generation and analysis of payloads at wire speed. Supports many PRBS patterns and user-defined patterns as payload. Report on error count, error rate, sync loss, SES, and others is provided.

- Capture data to file on individual ports, limited only by hard disk size

- Captures the traffic to files in SCF format

- PPP protocol analysis supported on single or multiple ports

- Memory based transmit/receive test with incremented sequence number based data for each packet

OC-12 / STM-4 PoS Analyzer

Alarms & Errors Counters Monitoring

- Monitored alarms and counters include –

  - ➢ Line errors such as OOF, LOS, LOF, AIS, RDI, and APSBF

  - ➢ FCS, Rx / Tx Abort, and MIN / MAX Length

  - ➢ Line, Path, and Section error counts
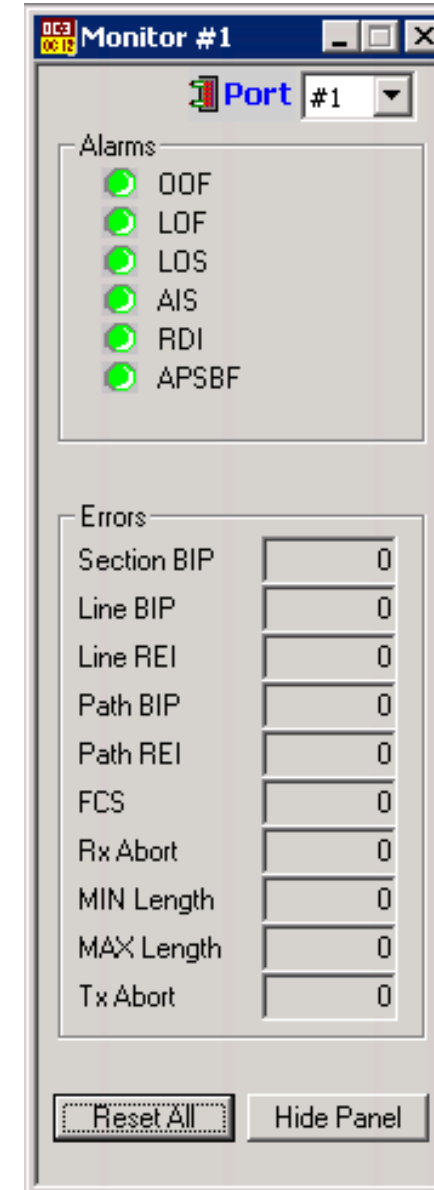
PoS Port Configuration

- Configure the FCS options at the transmission and reception side

- Rx FCS Bit Count - checks for 32bits, 16 bits, or no FCS value at the frame end

- Rx FCS Octets Present - allows the receiving side to strip the FCS octets from received PoS frames or to leave the FCS octets as received

- Tx Append FCS – allows adding the FCS octets at the end of every frame while transmitting

POS Port Configuration

Attribute	Port 1	Port 2	
Rx FCS Bit Count	32 bits	32 bits	
Rx FCS Octets Present	strip	strip	
Tx Append FCS	32 bits	32 bits	

Port 1
Port 2

32 bits
16 bits
none

Modify   Default   Exit

PoS Tx/Rx Test Features

- Option to send the fixed, random, or variable lengths test packets

- Insertion of a user-defined frame header in the packets transmitted

- Statistics display transmitted and received packet counts, packet errors and error distribution by the packet length

- Displays & allows to configure the bandwidth in Packets per second

- Categorizes the received sequence and data errors in different packet length groups called "Buckets". Each sequence error reported will be added to the corresponding bucket, there by updating the statistics

PoS Tx/Rx Test

PoS BERT Features

- BER application permits test to run over PPP, IP, or UDP layers

- User-defined header configuration

- User-defined traffic rate to the accuracy of 0.01% of total bandwidth

- Payload configuration to different PRBS patterns or user-defined patterns. User-defined pattern length can be 2 to 32 bits in length

- User-definable pre-sync achieve, sync loss bits, and sync loss declare options

- Supports sequence number insertion, invert payload data, single bit error insertion, and error rate insertion

- Provides detail statistics, such as Rx/Tx packet count, bit error count, IP and UDP checksum error count

- Provides throughput details, error and alarm LEDs for easy analysis

PoS BERT

PPP Protocol Analysis Features

- Capture packets over SONET/SDH

- Provide complete analysis of the protocol headers

- Supports filtering, statistics, remote connection via TCP/IP and many more functions

- Analyze PPP and higher layer data over the selected port(s)

- Supports a host of protocols PPP, IP, UDP, IPCP, BCP, BPDU, PAP, CHAP, HTTP, SNMP, STUN, FTP, DNS, and DHCP

- Ability to test and perform different analysis on received traffic

- Ability to test and analyze HDLC based PPP protocol in synchronous environment

- Summary view provides the information about few important fields (Port #, Layer 3 Protocol, LCP message type and higher protocol specific information like Destination and Source IP address, Destination and Source UDP port details, HTTP/FTP message type, etc)

- Ability to configure .INI file to customize sequence fragment format

PPP Protocol Analysis
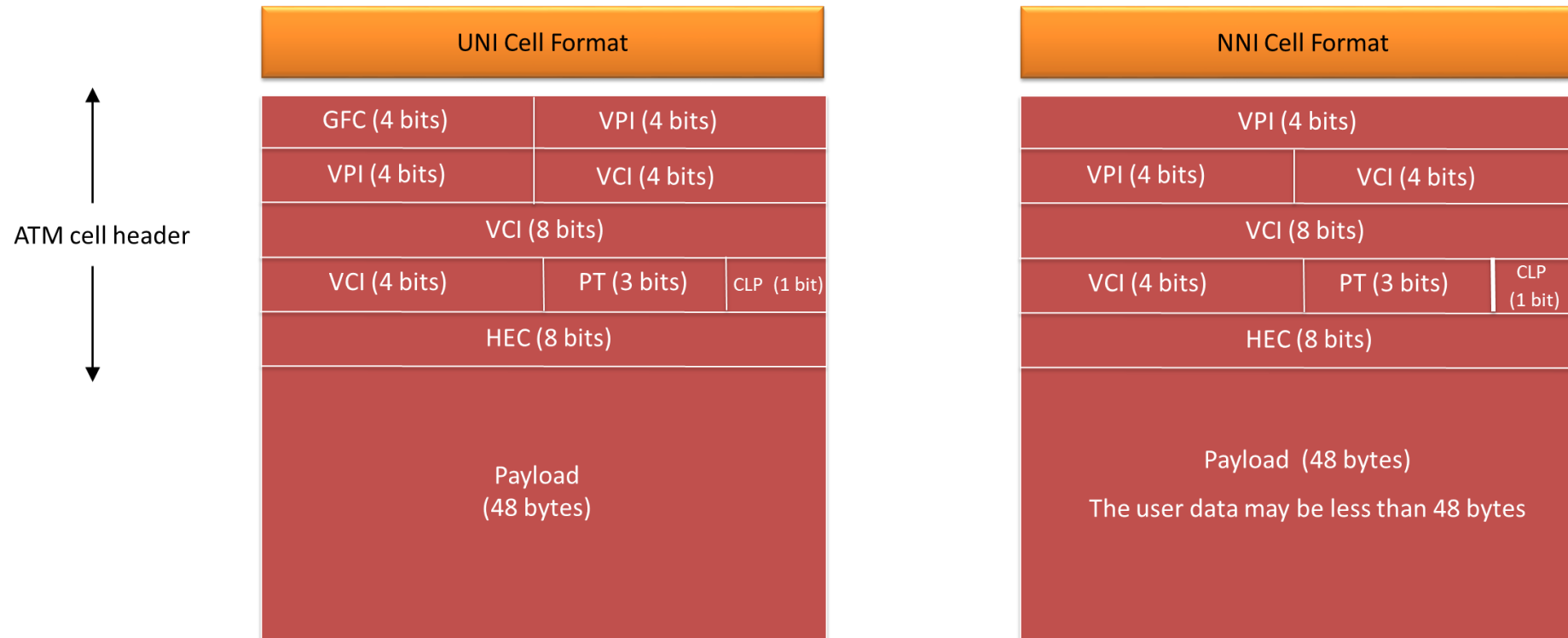
ATM - Asynchronous Transfer Mode

- LightSpeed1000™ complies with ITU-T ATM standards

- ATM layer architecture
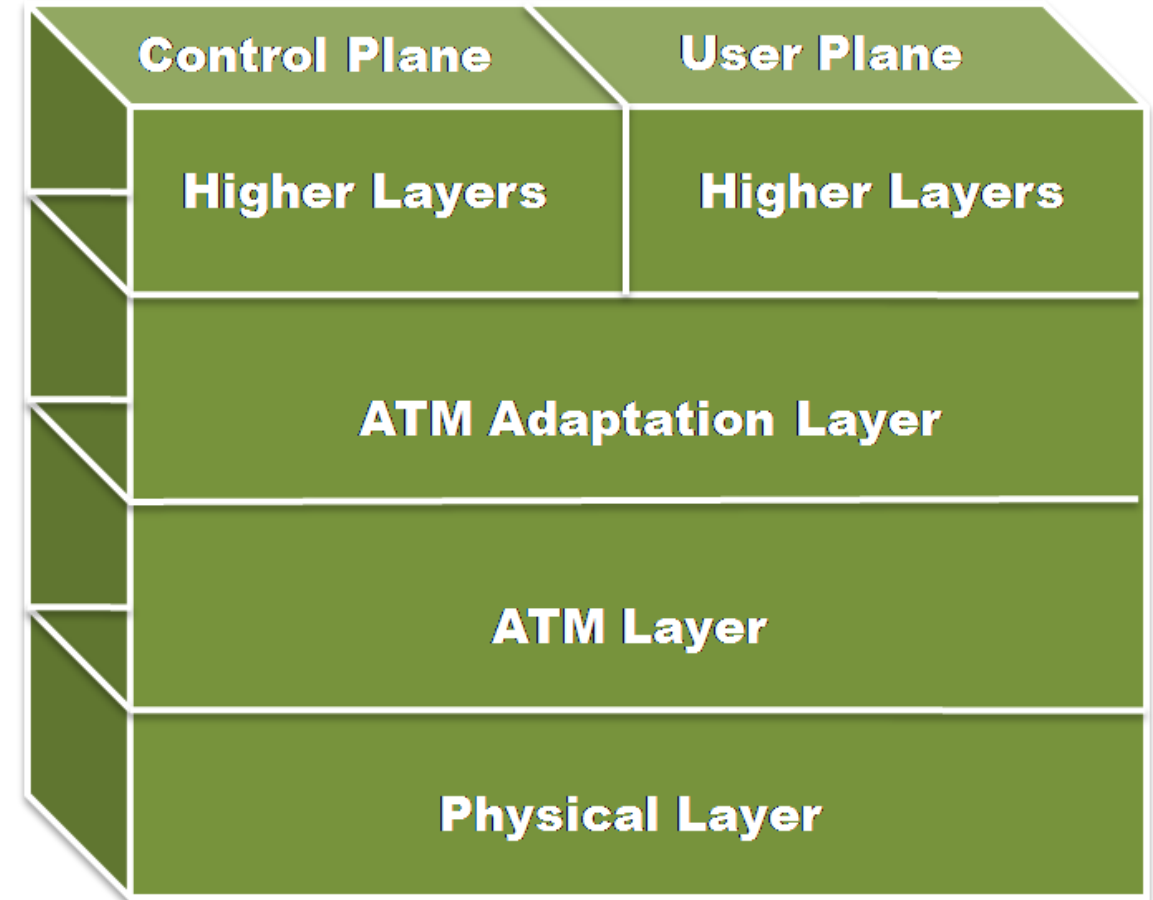
ATM Cell Structure in UNI and NNI Formats

- ATM network basically has two kinds of interfaces -
  - ➢ UNI (Interface between ATM User and Public ATM switch) and
  - ➢ NNI (Interface between two Public ATM switches)
- ATM Layer has Layer 2, ATM Adaptation Layer (AAL) as Layer 3 and other higher layers depending on C-Plane, U-Plane or Layer Management Plane

ATM cell header

UNI Cell Format	
GFC (4 bits)	VPI (4 bits)
VPI (4 bits)	VCI (4 bits)
VCI (8 bits)	
VCI (4 bits) / PT (3 bits) / CLP (1 bit)	
HEC (8 bits)	
Payload (48 bytes)	

NNI Cell Format	
VPI (4 bits)	
VPI (4 bits)	VCI (4 bits)
VCI (8 bits)	
VCI (4 bits) / PT (3 bits) / CLP (1 bit)	
HEC (8 bits)	
Payload (48 bytes) The user data may be less than 48 bytes	

Features

- Supports signal rates of 155.52 Mbps for OC-3 and 622.08 Mbps for OC-12 interface

- Emulation and analysis modes are supported on UNI or NNI per port

- Wire speed cell generation and processing on single or multiple ports using internal logic

- Capture data to file on individual ports, limited only by a hard disk size

- Comprehensive transmit/receive capabilities; transmitting and verifying with incrementing sequence numbers

- Simultaneous synchronous capture or transmit is possible on both optical ports

- ATM Tx/Rx application – Supports ATM traffic generation and cell analysis

- Ability to configure ATM headers (GFC, VPI, VCI, PT, and CLP fields), and bandwidth

- Rx cell analysis reports re-sync count errors and sequence errors

- Received cells hardware time stamping to the accuracy of 10ns

Features (Contd.)

- Loopback options : Supports Rx-to-Tx memory loopback, line loopback, diagnostic loopback, and PL3 loopback options

- Ability to capture real-time traffic and playback the traffic for simulation

- Complex and flexible hardware based filtering includes sixteen 128 bit independent filters with bit masks, for both ports with AND/OR include/exclude conditions

- ATM and UMTS protocol analysis supported on single or multiple ports

- Bit Error Rate Test module supports generation and analysis of payloads at wire speed. Supports ATM header configuration, PRBS patterns and user-defined patterns as payload. Report on error count, error rate, sync loss, SES, and others is provided

- SONET level statistics for both Tx and Rx cells. Additional statistics for errors, alarms, and BERT test cells

- Monitor and configure section, line, and path overhead bytes

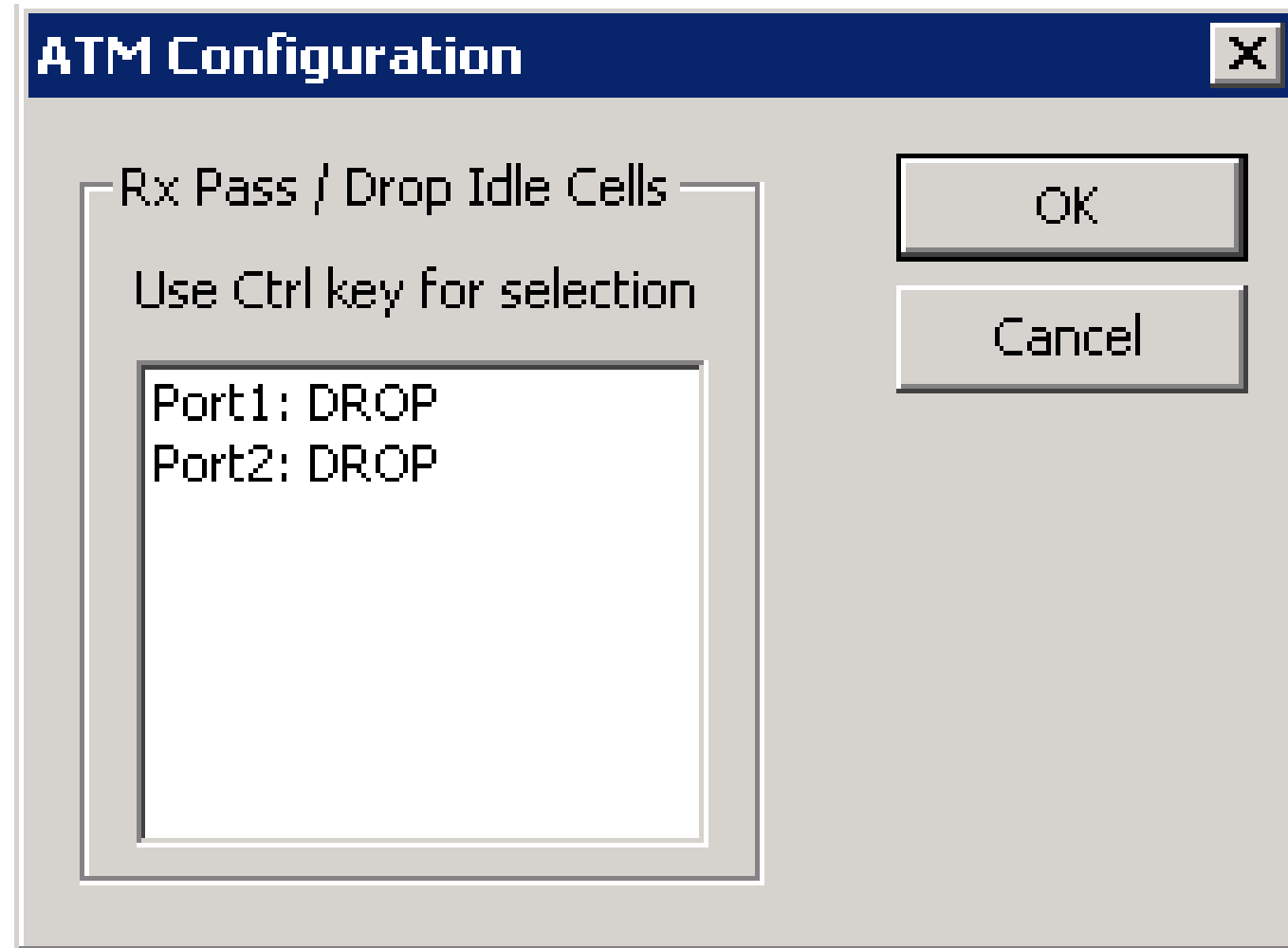# OC-12 / STM-4 ATM Analyzer

Alarms & Error Counters Monitor

- Alarms and error counts include –

  ➢ Line errors such as OOF, LOS, LOF, AIS, RDI, and APSBF

  ➢ Line, Path, and Section error counts
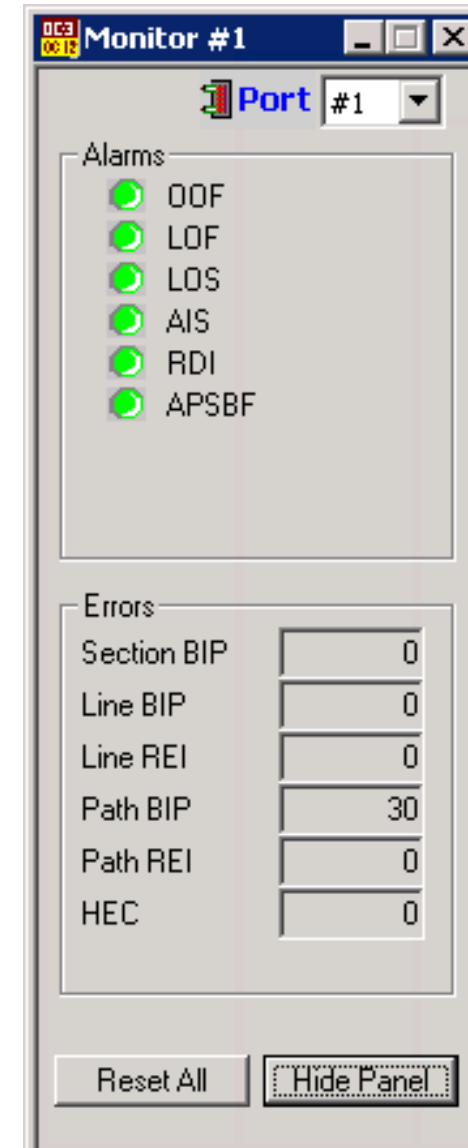
ATM Configuration

- ATM Configuration allows user to either pass or drop idle cells at the receiving stream

ATM Tx / Rx Test Features

- Generates ATM test cells and/or analyzes the received cells

- Transmit ATM cells with user configured ATM header bytes, bandwidth, and interface type (UNI/NNI)

- Generates test cells, which can be analyzed at the receiving end to check for data modifications and cell loss/insertion

- Sequence error can be inserted in the generated ATM cells using "Insert Error" feature.

- Tx configuration configures the bandwidth in cells per second

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ATM Tx/Rx Test

ATM BERT Features

- This application permits BER test to run as ATM payload

- User-defined header configuration supported

- User-defined traffic rate to the accuracy of 0.01% of total bandwidth

- Payload configuration to different PRBS patterns or user defined pattern. User defined pattern length can be 2 to 32 bits in length

- User definable pre-sync achieve, sync loss bits, and sync loss declare options

- Supports sequence number insertion, inverting payload data, single bit error insertion, and error rate insertion

- Provides detail statistics such as Rx/Tx cell count, idle cell count, bit error count, HEC error count

- Provides throughput details, error and alarm LEDs for easy analysis

ATM BERT

ATM Protocol Analysis Features

- ATM protocol analysis is used to capture ATM traffic

- Provide complete analysis of the protocol headers and reassembled PDUs along with call detail records

- Supports filtering, statistics, remote connection via TCP/IP and many more functions

- Analyze ATM frames received on selected port(s)

- Summary View displays Port #, Frame #, VPI/VCI, PT (Payload Type), HEC, OSF, AAL Type, Frame Type, CID, LI, CPI, UUI, SSSAR CID and SSCS message type and others

- Call trace capability based on UNI signaling parameters, VPI/VCI and others

- CRC verification for AAL5 carrying packet data

- Support of various UNI Signaling Protocols i.e. UNI 4.0, UNI 3.1 and UNI Q-2931

- Ability to configure .ini file for PVC carrying UNI signaling messages to get the proper decoding options

- Captures, decodes, filters, and reassembles (with or without Inverse Multiplexing option) AAL-2 and AAL-5 frames in real-time, from within the ATM cells according to user defined VPI/VCI

- Unscrambling of ATM cells based on SDH $X^{43} + 1$ algorithm

ATM Protocol Analysis

UMTS Protocol Analysis Features

- Analyze UMTS protocol headers over the selected port(s)

- Decodes different control plane protocols i.e. NBAP, RNSAP, RANAP, ALCAP, SSCOP, etc and user plane protocols i.e. Iu-UP, Iu-FP, AMR, etc

- Performs numerous measurements across Iub, Iur, IuCS, and IuPS interfaces

- Search and filtering capabilities for both real-time as well as offline analysis

- Decode NAS protocols (i.e. CC/MM/SM/SMS/GMM) along with the UTRAN specific protocols

- User can configure VPI/VCI values for PVCs carrying NBAP, RNSAP, RANAP, and ALCAP messages to enable decoding of the said protocols

- Ability to configure .ini file for VPI & VCI (for ALCAP, NBAP, RANAP, and so on)

- CRC verification for AAL5 carrying packet data

- Unscrambling of ATM cells based on SDH X^43 + 1 algorithm

- Captures, decodes, filters, and reassembles AAL-2 and AAL-5 frames (with or without Inverse Multiplexing option) from within the ATM cells according to user-defined VPI/VCI

- Call trace capability over IuCS and IuPS interfaces

UMTS Protocol Analysis

Common Applications in ATM & PoS Analyzers

Tx Packets (Cells) from File

Tx Packets (Cells) from File

- Transmits packets / cells from the file

- Packets can be transmitted either continuously, limited by number of packets/cells, or till the end of file (EOF)

- Transmit packets/cells at a user configurable rate

- Transmits on the same port as captured, swaps ports or uses a specified port

- Provides the statistics of the transmitted cells at both line level and payload level

- Synchronous Multi-Board option allows to transmit packets synchronously on multiple boards

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Rx Packets to File

- Captures the received packets and saves them into a file

- Packets can be captured continuously (till user manually stops the capture) or limited by a specified size in MB, a packet count, or a specified time limit

- Synchronous Multi-Board option allows to capture incoming packets synchronously on multiple boards

Rx-to-Tx Memory Loopback

Software Loopback
(Rx-To-Tx Memory Loopback)

- Software loopback is used for diagnostic purposes

- It loops all the received packets / cells from the SONET to the transmitting ports

- Selection of source and destination ports to transmit and receive packets/cells

- Selection of ports on different boards for Tx and Rx, where multiple boards are used in a single chassis

- Display of the Tx and Rx information

- Loop back the data either in the page mode, 4K bytes at a time, or in the packet mode, packet by packet

- In Packet Mode Flush Tx option ensures that the packet goes out without any delay

RAW or Transparent Mode

- Raw or transparent mode allows direct access to the SONET / SDH payload for BERT, data transmit and receive applications

- RAW BERT - support for the following PRBS Patterns: $2^9 - 1$, $2^{11} - 1$, $2^{15} - 1$, $2^{20} - 1$, $2^{23} - 1$, $2^{29} - 1$, $2^{31} - 1$, all one's, all zero's, alternate ones and zeros, user-defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^{-1} to 10^{-9}, status for pattern sync, and bit errors counters

- Wirespeed capture of raw data to hard disk on both ports simultaneously

- Alarms and Error (section, path, and line) monitoring and logging

- Multi-stage loopback – Supports Rx-to-Tx memory loopback, line loopback, diagnostic loopback, and PL3 loopback options

Filtering Options

- Supports setting different filtering options at the hardware level feature

- Filtering done on a combination of multiple conditions or single condition
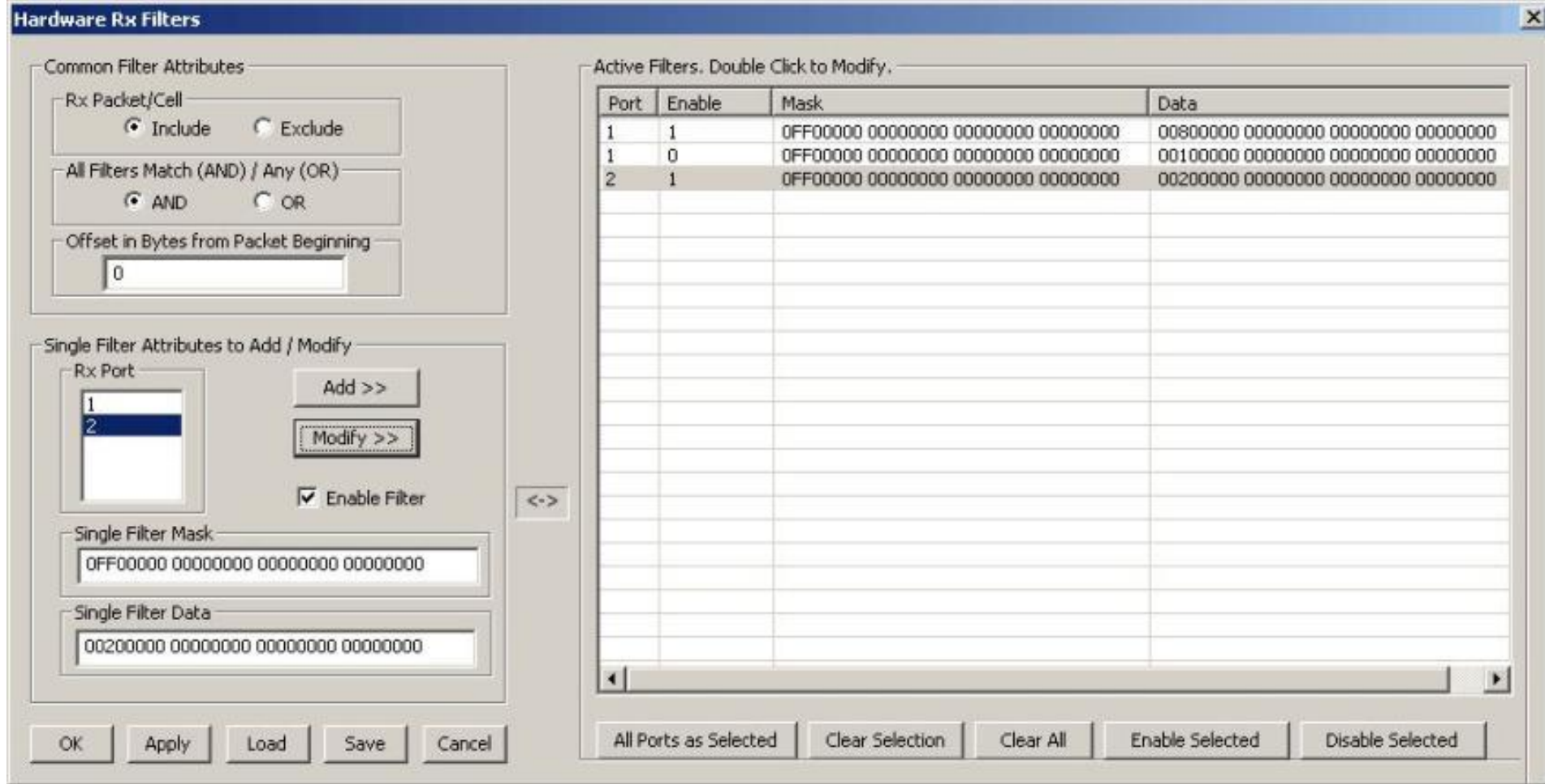
Packet Delay Emulation

Overview

- Combines hardware and software-based functions to achieve precision and flexibility

- Provides full duplex delay simulation for PoS and ATM based traffic from 1 ms to 500 ms, with incremental delays of 1 ms

- Emulate packet delays that occur over SONET/SDH carrying ATM/PoS traffic

Working Principle

- Payload received on Port 1 is delayed by the application with the applied delay in milliseconds and transmitted back on to Port 2

- Data received on Port 2 will be transmitted back on to Port 1 with applied delay. The applied delay duration is same for both the ports
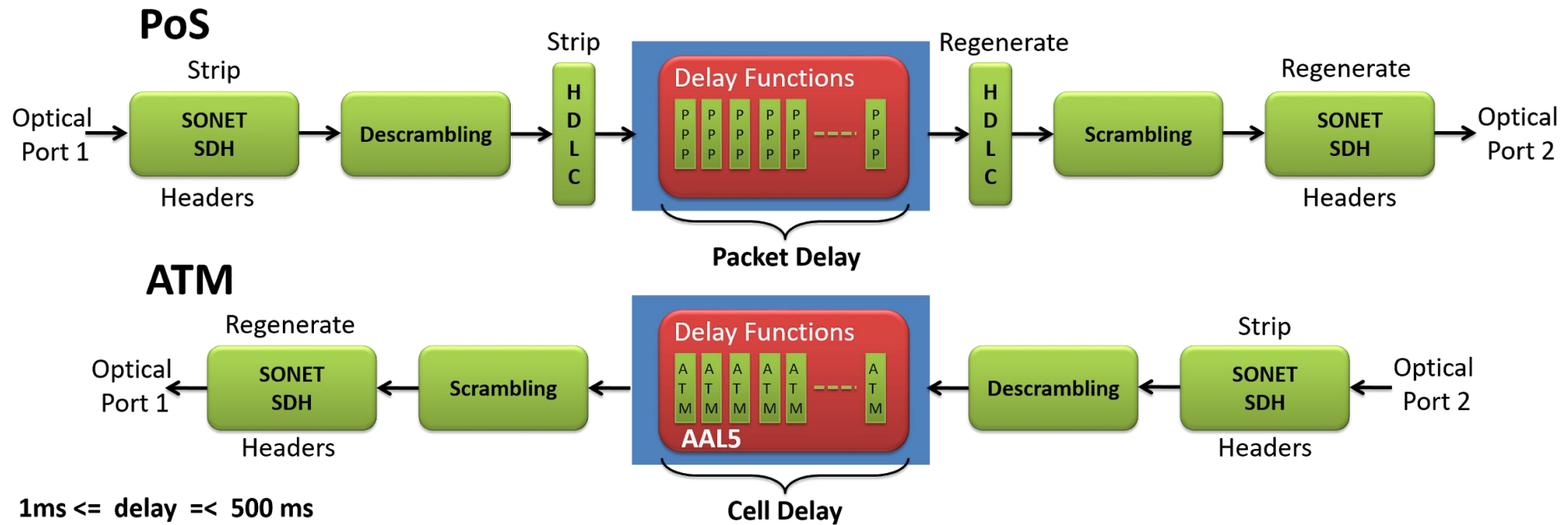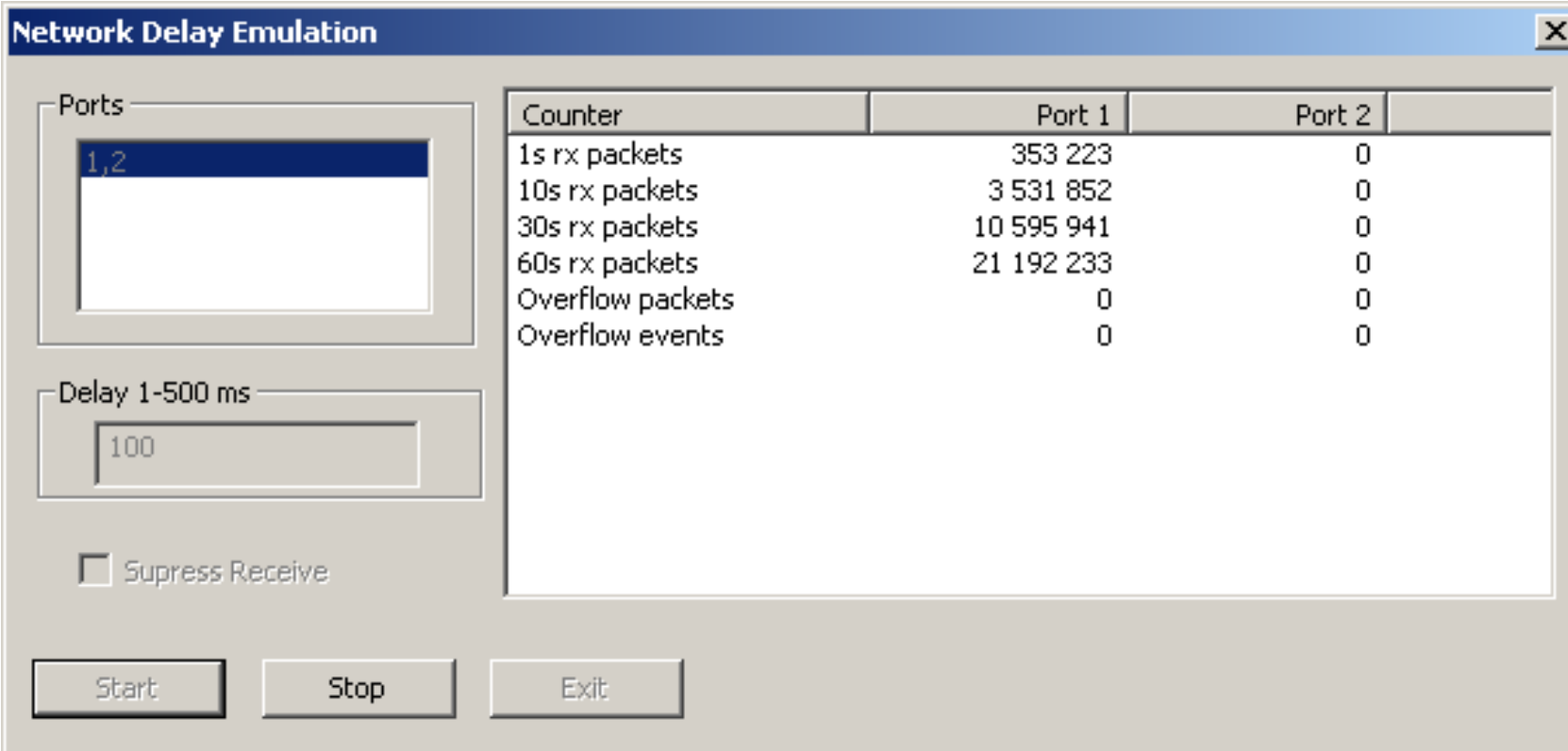

1ms <= delay =< 500 ms
programmable in 1 ms increments

What does this application do?

- With this application, the user can:

  ➢ test the impact of delay and congestion under various real world conditions

  ➢ assess impact of delay on SLA (Service Level Agreements)

  ➢ simulate satellite delay and long Fiber Loops

  ➢ test WAN application performance under deteriorated but repeatable conditions

Network (Packet) Delay Emulation

- Ports
  - ➢ Allows to apply the delay simultaneously for the incoming packets on both ports

- Delay 1–500ms
  - ➢ User can introduce the delay from 1 ms to 500ms. Minimum delay is 1ms and minimum programmable incremental delay is 1ms

Thank you